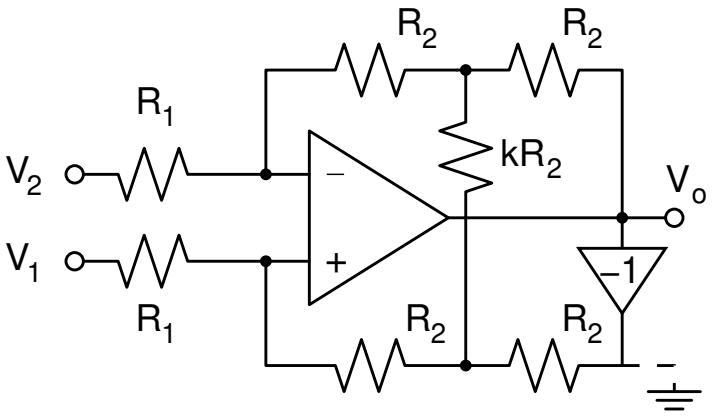
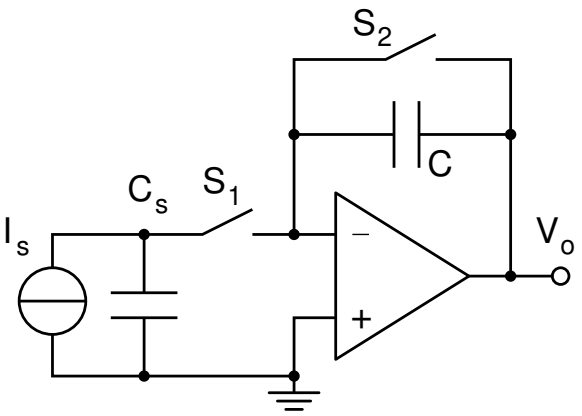
Electronics – February 15 2017 Prof. A. Spinelli





Problem 1

The scheme in the left figure is a subtractor circuit with adjustable gain (consider the scheme without the ground connection). The amplifier has $A_o = 120$ dB and two poles, at 1 and 10^5 Hz. Hint: *exploit the circuit symmetry and the common-mode/differential-mode representation of the inputs whenever possible*.

1. Find the closed-loop gain of the stage.
2. Compute the loop gain of the stage in the simplified case of $R_1 = R_2$ and find the condition on k that ensures stability (e.g., phase margin larger than 45°).
3. Compute the rms output voltage noise when the OA has $\sqrt{S_V} = 10$ nV/$\sqrt{\text{Hz}}$ and $R_1 = R_2$, $k = 0.11$.
4. Disconnect the inverting buffer and connect the lower-right resistor R_2 to ground (dashed line). What is the new gain of the stage?

Problem 2

A sensor is schematized by a current source and its parallel capacitance $C_s = 1$ pF (Fig. on the right) and noise current source $\sqrt{S_n} = 10$ pA/$\sqrt{\text{Hz}}$. The amplifier is connected as a gated integrator, controlled by the switches S_1 and S_2. The integration capacitor is $C = 100$ pF.

1. Compute the value of the integration time that allows to measure a DC current source of 1 nA with $S/N = 10$.
2. OA has $GBWP = 10$ MHz. Find the condition on its voltage and current noise sources for them to be negligible.
3. Open and closed switches can be described by high- or low-value resistors, having their own thermal noise ($4k_BT \approx 1.646 \times 10^{-20}$ J). Consider the integration phase and find the condition on resistor values that do not modify S/N.
4. Consider a delta-like input signal, $I_s = Q\delta(t)$. Due to a sinchronization error, S_1 closes just *after* the input pulse. What happens to the output signal and noise? What if we consider an equivalent resistor R_s in parallel to C_s?

Question

Describe the Boxcar Averager working principle and the number of equivalent samples.

For a correct evaluation, you are asked to write your answers in a readable way; thank you

Do a good job!

Results will be posted by February 17th **Mark registration: Monday, Feb 20th**

Solution

Problem 1

1.1

We follow the suggestion and split the input into the sum of a common-mode voltage V_C and a differential-mode voltage V_D. When V_C is applied to both inputs, it is easy to see that no current can flow into the resistor kR_2, because of the symmetry of the circuit. The non-believer can simply note that the same current must flow from the input into the two resistors R_1, to keep $V^+ = V^-$. This in turn means that resistors R_2 will experience the same voltage drop, and that the same voltage is present at the two ends of the resistor kR_2. Since no current flows in it, we can safely remove it without altering the circuit behavior, and we immediately realize that V_o must be equal to zero.

Moving to the differential-mode transfer, we could note that the circuit is perfectly antisymmetric, so that the midpoint of the bridge resistor kR_2 must be at zero voltage, and so must be the input voltages of the OA (they must satisfy $V^+ = -V^-$ because of antisymmetry, and $V^+ = V^-$ because of the ideal OA operation). We can then follow the half-circuit approach, in analogy with the instrumentation OA calculations, solving the much simpler circuit in Fig. 1 (left). The voltage between the two resistors R_2 is at a bias $V_A = (R_2/R_1)V_D/2$ and the KCL reads:

$$\frac{V_A - V_o}{R_2} + \frac{2V_A}{kR_2} + \frac{V_A}{R_2} = 0,$$

from which we get

$$V_o = 2V_A\left(1 + \frac{1}{k}\right) = \left(1 + \frac{1}{k}\right)\frac{R_2}{R_1}V_D.$$

Clearly, changing the value of the bridging resistor kR_2 allows to modify the gain of the differential stage withour offsetting the resistor balance, i.e., without modifying the CMRR.

1.2

When the loop is broken at the OA output, we can see that the circuit remains antisymmetric. Hence, we can use the half-circuit to compute G_{loop}, but we need to keep in mind that now it is not true that $V^+ = V^-$, and we can only say that $V^+ = -V^-$. If $R_1 = R_2$ it is easy to see that voltage V_A is now

$$V_A = V_s\frac{2R \parallel (k/2)R}{R + 2R \parallel (k/2)R} = V_s\frac{2k}{3k+4}.$$

From V_A, we immediately have

$$V^+ = \frac{V_A}{2} = V_s\frac{k}{3k+4}$$

and, obviously, $V^- = -V^+$. Hence:

$$G_{loop} = -A(s)\frac{2k}{3k+4}.$$

For the phase margin to be larger than 45°, f_{0dB} must fall at the second pole frequency, i.e., 100 kHz. $A(s)$ must then be lowered by a factor of ten, which means:

$$\frac{2k}{3k+4} < \frac{1}{10} \Rightarrow k < \frac{4}{17} \approx 0.235 \Rightarrow G_{id} > 5.25.$$

1.3

We take advantage once again of the symmetry and split the voltage V_n into the sum of two sources $V_n/2$ in series at each input of the OA (which give zero contribution) and a differential noise voltage $\pm V_n/2$ in series at the same inputs. Now, we just solve the half-circuit in Fig. 1 (left) with noise voltage $V_n/2$ located at the non-inverting input of the OA. V_A is now equal to $V_n(R_1 + R_2)/2R_1$ and the KCL becomes:

$$V_A\frac{2}{kR_2} + \frac{V_n}{2R_1} + \frac{V_A - V_o}{R_2} = 0 \Rightarrow V_o = V_n\left[\frac{1}{2} + \frac{R_2}{R_1} + \frac{1}{k}\left(1 + \frac{R_2}{R_1}\right)\right].$$

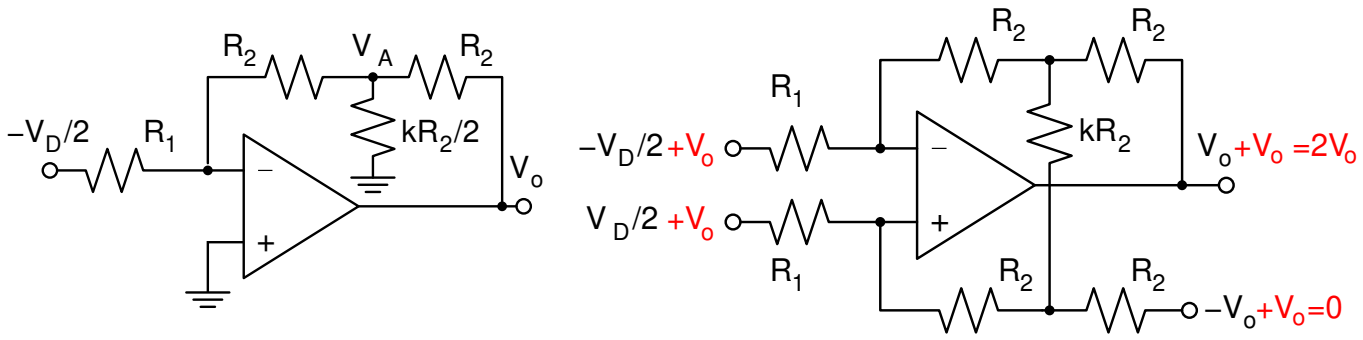


Figure 1: Left: Half circuit used for gain calculation. Right: Node voltages when a term V_o is added at each circuit node to mimic the grounded amplifier.

Under the specified conditions the gain becomes ≈ 19.7 and $f_{0dB} = 50$ kHz. The output rms noise is simply:

$$\overline{V_o^2} = S_V \; 19.7^2 \; \frac{\pi}{2} f_{0dB} \approx (55 \; \mu\text{V})^2.$$

1.4

It is easy to see that the stage remains a differential amplifier, with common-mode gain equal to zero. Let's now find the new differential gain, first with (boring) calculations and later with a clever reasoning. Calling V_A and V_B the voltages at the higher and lower end of resistor kR_2, we equal the voltage at the input pins of the OA, obtaining:

$$V_A \frac{R_1}{R_1+R_2} - \frac{V_D}{2}\frac{R_2}{R_1+R_2} = V_B \frac{R_1}{R_1+R_2} + \frac{V_D}{2}\frac{R_2}{R_1+R_2} \Rightarrow V_A - V_B = V_D \frac{R_2}{R_1},$$

and the current in the bridge resistor is V_D/kR_1. The voltage V_B can be found by the KCL at the node at the lower end of the bridge resistor:

$$\frac{V_D/2 - V_B}{R_1+R_2} + \frac{V_D}{kR_1} = \frac{V_B}{R_2} \Rightarrow V_B = V_D \frac{R_2}{R_1}\frac{R_1(k+2)+2R_2}{2k(R_1+2R_2)},$$

and obviously

$$V_A = V_B + V_D\frac{R_2}{R_1} = V_D \frac{R_2}{R_1}\frac{R_1(3k+2)+R_2(4k+2)}{2k(R_1+2R_2)}.$$

The KCL at the V_A node gives us V_o:

$$\frac{V_1 + V_D/2}{R_1+R_2} + \frac{V_D}{kR_1} = \frac{V_1 - V_0}{R_2} = 0 \Rightarrow V_o = 2V_D\frac{R_2}{R_1}\left(1+\frac{1}{k}\right),$$

which is two times the result obtained in 1.1. Let's see if we could have reached this result without calculations: we start from the initial configuration of the amplifier, represented as in Fig. 1 (left) and add a voltage equal to V_o to each node. Clearly, we are now in the requested configuration with the grounded node, while the output has doubled. Of course, we have the additional term V_o at the input, but this is of no concern to us, *because the common-mode gain is still zero* and this term will give no contribution to the output.

Problem 2

2.1

The expression for the signal-to-noise ratio of the gated integrator is

$$\frac{S}{N} = \frac{I_s}{\sqrt{S_n/2T_G}} = 10 \Rightarrow T_G = \frac{100 S_n}{2I_s^2} = 5 \text{ ms}.$$

2.2

The noise current source is in parallel with S_n, so it suffices to say $S_I \ll S_n$, which means a CMOS OA should be picked. The noise voltage source, instead, gives an output PSD equal to

$$S_{V_o} = S_V \left(1 + \frac{C_s}{C}\right)^2 \approx S_V,$$

meaning that we need to consider the pole introduced by the OA, resulting in

$$\overline{V_o^2} = S_V \frac{\pi}{2} GBWP.$$

Note that even when S_2 is closed, a noise PSD equal to S_V exists at the output: this noise is *not* affected by the gated integrator operation, and this is why its pole does not come into play. For this noise to be negligible, we set

$$S_V \frac{\pi}{2} GBWP \ll S_n \frac{T_G}{2C^2} \Rightarrow S_V \ll S_n \frac{T_G}{\pi C^2 GBWP} = 1.6 \times 10^{-12} \text{ V}^2/\text{Hz},$$

i.e., $\sqrt{S_V} \ll 1.3\ \mu\text{V}/\sqrt{\text{Hz}}$, easily satisfied.

2.3

Switch resistors affect both signal and noise, so we should consider both. Let us start with the signal: the off resistance of S_2 creates an LPF with the integration capacitor C, while the on resistance of S_1 creates an LPF with capacitor C_s. The first time constant must be much greater than T_G, while the second must be much smaller:

$$CR_H \gg T_G \Rightarrow R_H \gg T_G/C = 50\ \text{M}\Omega$$
$$C_s R_L \ll T_G \Rightarrow R_L \ll T_G/C_s = 5\ \text{G}\Omega.$$

We now consider the noise of S_2, replacing it (during the integration phase) with a resistor R_H having thermal noise PSD $S_{I_R} = 4k_BT/R_H$. Because $CR_H \gg T_G$, this noise is integrated like the sensor noise, so that we can then simply put

$$\frac{4k_BT}{R_H} \ll S_n \Rightarrow R_H \gg \frac{4k_BT}{S_n} = 160\ \Omega,$$

which is obviously not a concern. The closed switch S_1 is better represented by its voltage noise source $S_{V_R} = 4k_BTR_L$, which gives an output noise equal to:

$$S_{V_o} = S_{V_R} \left| \frac{sC_sR_H}{(1 + sCR_H)(1 + R_LC_s)} \right|^2 \approx S_{V_R} \left| \frac{C_s/C}{1 + R_LC_s} \right|^2,$$

because of the very low frequency R_HC pole. This is a low-pass filter with time constant $R_LC_s \ll T_G$, meaning that the gated-integrator has basically no effect on the noise. We then have

$$\overline{V_o^2} = S_{V_R} \left(\frac{C_s}{C}\right)^2 \frac{1}{4R_LC_s} = k_BT \frac{C_s}{C^2},$$

which is independent of R_L. This noise is also much smaller than the input one, as we can easily check:

$$k_BT \frac{C_s}{C^2} \ll S_n \frac{T_G}{2C^2} \Rightarrow T_G \gg \frac{2k_BTC_s}{S_n} \approx 80\ \text{ps}.$$

In this case, it is clearly the signal requirement that sets the resistor values.

2.4

in the first case, everything is the same. When S_1 is open, the charge Q is stored onto the capacitor C_s and later transferred to the capacitor C when the switch is closed. The output voltage becomes then Q/C, while the noise is of course only dependent on the integration time.
If the parallel resistance is finite, C_s will discharge with time constant C_sR_s and the output signal will be degraded accordingly.