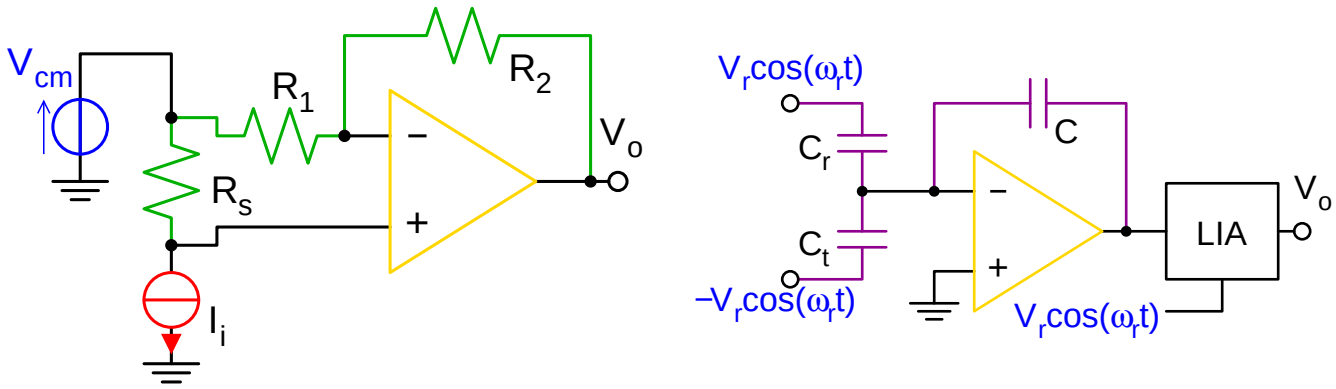
Electronics – September 10 2018 Prof. A. Spinelli



Problem 1

The scheme in the left figure is a current monitor (V_{cm} is a common-mode voltage). Component values are $R_1 = 10\ \Omega$, $R_2 = 1\ \text{k}\Omega$, $R_s = 0.01\ \Omega$. The OA has $A_o = 130$ dB and $GBWP = 10$ MHz.

1. Find the expression of the output voltage. Why aren't we using a simple $I - V$ converter?
2. The OA has input capacitance equal to 32 pF (differential mode) and 8 pF (common mode). The input resistance is 30 kΩ (differential mode) and 50 MΩ (common mode). Discuss the stability of the stage.
3. Compute the output rms noise voltage considering the equivalent noise sources of the OA, $\sqrt{S_V} = 1\ \text{nV}/\sqrt{\text{Hz}}$ and $\sqrt{S_I} = 3\ \text{pA}/\sqrt{\text{Hz}}$, plus the resistor noise ($4k_BT \approx 1.646 \times 10^{-20}$ J).
4. Find a solution to eliminate the effect of the common-mode voltage V_{cm} (you can use multiple OAs).

Problem 2

The scheme in the right figure employs an LIA and an amplifier with a reference capacitor $C_r = 2$ pF to measure the value of a test capacitor $C_t = C_r + \Delta C$. The OA has input noise voltage PSD $S_V = K/f$ with $K = 10^{-10}\ \text{V}^2$ and $C = 0.5$ pF. Consider $V_r = 1$ V.

1. We want to measure $\Delta C \approx 0.1$ fF. Find a set of values for the LIA parameters considering that the measurement must be completed in 10 ms.
2. Find the condition on the OA offset voltage and (white) noise current PSD for them to not degrade S/N. Repeat the problem for the flicker component.
3. Because of a gain error, the amplitude of the negative reference signal is now $-(V_r + \Delta V)$. Evaluate the effect on the output signal.
4. There are parasitic resistors R_t and R in parallel to C_t and C. Consider first each of them separately and then together and find the condition for them not to degrade S/N (carefully consider the signal phases).

For a correct evaluation, you are asked to write your answers in a readable way; thank you

Do a good job!

Results will be posted by September 13th **Mark registration: Friday, Sep. 14th**

Solution

Problem 1

1.1

By application of the linear superposition principle and elementary calculations, we get

$$V_o = V_{cm} - I_i R_s \left(1 + \frac{R_2}{R_1}\right).$$

Note that the transresistance of the stage is nearly 1 Ω, allowing to measure large currents (for example, if the output dynamics is ±10 V and V_{cm} is small, the input range is ±10 A). With a simple $I - V$ converter, this current has to be sourced/sinked by the power OA. Here, instead, we can use an OA optimized for low noise and low offset, increasing the precision.

1.2

Let's start with some reasoning: the "ideal" transfer without any parasitic element would give a closed-loop bandwidth of about 100 kHz. So, any singularity well beyond that value can be neglected. Now, CM input resistances can be dropped, as they are in parallel to either R_s or R_1 (and R_2, but that's much bigger). The impedance given by $R_s \parallel C_c$ can also be neglected, given its very low value (10 mΩ with a pole at 2 THz). We are then left with a capacitance given by the parallel of C_d and C_c and a resistance nearly equal to R_1, yielding a pole in the loop gain at:

$$f_p \approx \frac{1}{2\pi(C_c + C_d)R_1} = 397 \text{ MHz},$$

clearly irrelevant. If you are passionate about analytical solutions, you can look at Fig. 1 (left) where the full scheme is shown and where $Z_1 = R_1 \parallel R_c \parallel C_c \approx R_1 \parallel C_c$, $Z_d = R_d \parallel C_d$ and $Z_s = R_s \parallel R_c \parallel C_c \approx R_s \parallel C_c$. We easily obtain for the differential input voltage

$$-V_d = \frac{Z_1 \parallel (Z_d + Z_s)}{R_2 + Z_1 \parallel (Z_d + Z_s)} \frac{Z_d}{Z_d + Z_s} = \frac{Z_1 Z_d}{R_2(Z_1 + Z_d + Z_s) + Z_1(Z_d + Z_s)}.$$

After elementary but tedious manipulations, and considering that R_s is much smaller than any other resistance and can be neglected, we obtain the equation providing the poles:

$$s^2 R_1 R_2 R_d R_s (2C_d C_c + C_c^2) + s R_1 R_2 R_d (C_d + C_c) + R_1 R_2 + R_d(R_1 + R_2) = 0,$$

giving a low-frequency pole at

$$s \approx -\frac{R_1 R_2 + R_d(R_1 + R_2)}{R_1 R_2 R_d (C_d + C_c)} \approx -\frac{1}{R_1(C_d + C_c)}.$$

1.3

Representing resistor noise via their current sources, we can group them into two sources at the OA input, having values

$$S_I^+ = S_I + \frac{4k_B T}{R_s} = 9 \times 10^{-24} + 1.6 \times 10^{-18} \approx 1.6 \times 10^{-18} \text{ A}^2/\text{Hz};$$
$$S_I^- = S_I + \frac{4k_B T}{R_1} + \frac{4k_B T}{R_2} = 9 \times 10^{-24} + 1.6 \times 10^{-21} + 1.6 \times 10^{-23} \approx 1.6 \times 10^{-21} \text{ A}^2/\text{Hz}.$$

Note the low current noise of the OA, much smaller than the resistor contributions. The final PSD becomes then:

$$S_{V_o} = (S_V + S_I^+ R_s^2)\left(1 + \frac{R_2}{R_1}\right)^2 + S_I^- R_2^2 = (10^{-18} + 1.6 \times 10^{-22})101^2 + 1.6 \times 10^{-15} \approx \left(100 \text{ nV}/\sqrt{\text{Hz}i}\right)^2,$$

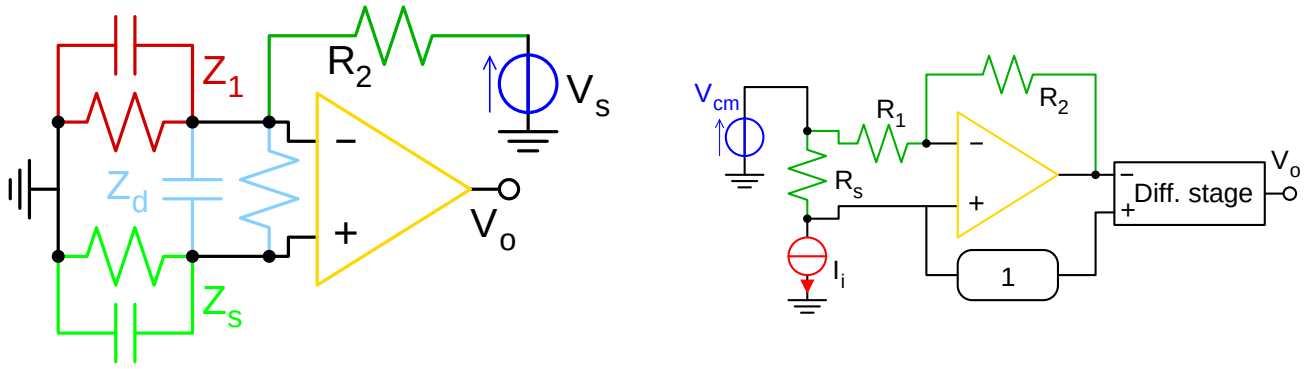


Figure 1: Left = Full scheme for G_{loop} calculation. Right = Possible scheme for V_{cm} compensation.

dominated by the voltage noise of the OA. Considering a closed-loop bandwidth of 100 kHz, we obtain the rms noise:

$$\sqrt{\overline{V_o^2}} = 10^{-7}\sqrt{\frac{\pi}{2}10^5} \approx 40\ \mu\text{V}.$$

1.4

The easiest solution is probably to buffer V_{cm} and subtract it from the output. A possible scheme is outlined in Fig. 1 (right). Note that the transresistance gain is now exactly $R_s(R_2/R_1)$.

Problem 2

2.1

The LIA input signal amplitude is

$$x(t) = V_r\frac{C_t - C_r}{C} = V_r\frac{\Delta C}{C},$$

while the (unilateral) input noise PSD is

$$S_x = S_V\left(1 + \frac{C_r + C_t}{C}\right)^2 \approx \frac{K}{f}\left(1 + \frac{2C_r}{C}\right)^2,$$

leading to

$$\left(\frac{S}{N}\right) = \frac{V_r\Delta C}{2C_r + C}\sqrt{\frac{f_r}{2KBW_n}},$$

where f_r is the reference frequency. The output signal is controlled by the time constant of the LIA LPF. If the signal is to be stable in 10 ms, the time constant must be smaller than about 2 ms, so let's take it to be $\tau = 1$ ms, i.e., $BW_N = 1/4\tau = 250$ Hz. We then get $f_r \approx 101$ Hz. However, f_r must be significantly larger than the LPF bandwidth (160 Hz) for it to reject the harmonics at $2f_r$, so it is wise to raise it to – say – 1.5 kHz.

2.2

The offset voltage is a DC value and does not affect the measurement (unless it saturates the stage, which is not our case). The LIA input noise PSD due to the OA current noise is instead

$$S_x = S_I\frac{1}{(\omega C)^2}$$

and it is negligible if

$$\frac{S_I}{(2\pi f_r C)^2} \ll \frac{K}{f_r}\left(1 + \frac{2C_r}{C}\right)^2 \Rightarrow S_I \ll K(2C_r + C)^2 4\pi^2 f_r \approx 10^{-28}\ \text{A}^2/\text{Hz}.$$

Note that this means $\sqrt{S_I} = 10$ fA/$\sqrt{\text{Hz}}$; a low-noise CMOS OA is required. The requirement on the flicker noise simply means that the noise corner fequency must be lower than f_r.

2.3

The input voltage to the LIA is now

$$x(t) = \frac{(V_r + \Delta V)(C_r + \Delta C) - V_r C_r}{C} \approx \frac{V_r \Delta C + C_r \Delta V}{C},$$

generating an extra contribution. We must therefore have

$$C_r \Delta V \ll V_r \Delta C \Rightarrow \Delta V \ll V_r \frac{\Delta C}{C} = 0.2 \text{ mV}.$$

A good precision is hence required. Note that this error can be measured and subtracted if a precisely known test capacitor is available. The problem becomes then – as usual – the drift in ΔV.

2.4

The current flowing into the resistor R_t generates an input signal of amplitude $V_r/\omega_r C R_t$ that is out of phase by -90° with respect to the modulated current, and will *not* generate any error on the signal! However, such resistor will also contribute to the noise, degrading S/N. If we describe the resistor noise via its current source (placed in parallel to the current noise of the OA), we can exploit the result in 2.2 and obtain:

$$\frac{4k_B T}{R_t} \ll 10^{-28} \Rightarrow R_t \gg 160 \text{ M}\Omega.$$

The same considerations for the noise hold for R. When accounting for the signal, instead, the transfer function becomes:

$$T(s) = \frac{s\Delta C R}{1 + sCR},$$

and we must now set

$$\omega_r CR \gg 1 \Rightarrow R \gg \frac{1}{2\pi C f_r} \approx 200 \text{ M}\Omega.$$

When we have both resistors in place, the transfer function to the LIA input becomes

$$T(s) = \frac{R}{R_t} \frac{1 + s\Delta C R_t}{1 + sCR},$$

and we get once again errors in magnitude and phase. In principle, the simplest solution is just to set

$$\omega_r CR \gg 1 \Rightarrow R \gg \frac{1}{2\pi C f_r} \approx 200 \text{ M}\Omega,$$

which means that we can neglect the "1" at the denominator and fall back to the first case, with no effect on the signal and no condition on R_t.

In reality, however, things a just a bit more complicated because of delays. *If we account for all propagation delays and adjust the phase of the LIA reference to get the maximum output, as is usually done*, the output signal will be related to the magnitude of $T(j\omega_r)$, and we must now include the error at the numerator, setting:

$$\omega_r \Delta C R_t \gg 1 \Rightarrow R_t \gg \frac{1}{2\pi \Delta C f_r} \approx 1 \text{ T}\Omega.$$

The value can be somewhat reduced by increasing the modulation frequency.