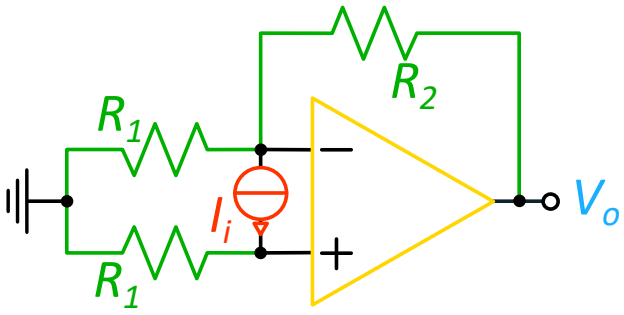
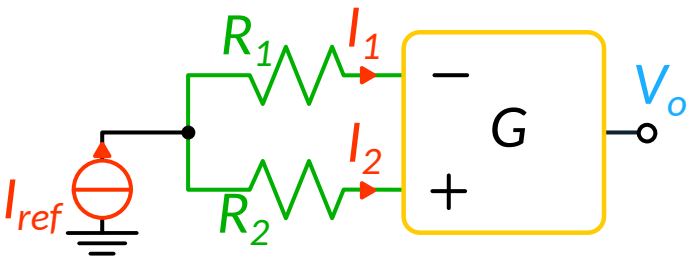
Electronics – January 21 2022 Prof. A. Spinelli





For a correct evaluation, please write your answers in a readable way; thank you!

Problem 1

The scheme in the left figure is a transresistance amplifier. Parameter values are $R_1 = 1.3$ MΩ, $R_2 = 5.6$ MΩ. The low-voltage OA has low-frequency gain of 40 V/mV and $GBWP = 2$ MHz.

1. Find the the closed-loop gain in the ideal case.
2. The OA has a differential input capacitance $C_i = 2$ pF. Compute the loop gain and compensate the stage if needed (do not change the value of resistors).
3. Compute the output rms noise voltage considering the equivalent noise source of the amplifier $\sqrt{S_V} = 10$ nV/$\sqrt{\text{Hz}}$.
4. The circuit is powered by a single-supply source $V_{cc} = 5$ V. Add the necessary biasing elements to the circuit.

Problem 2

The scheme in the right figure is a current-mode Wheatstone bridge, where $I_{ref} = 1$ mA and the two resistive sensors are $R_1 = R(1 + x)$ and $R_2 = R(1 - x)$ with $R = 100$ Ω. The differential transresistance amplifier sets $V_o = G(I_2 - I_1)$, keeping its input pins at the same bias. Its input noise PSDs are $\sqrt{S_I} = 7$ nA/$\sqrt{\text{Hz}}$, $\sqrt{S_V} = 100$ nV/$\sqrt{\text{Hz}}$, and the bandwidth is 10 kHz.

1. The maximum value of x is 10% and the output voltage must vary in the range $0 - 5$ V. Find the corresponding value of G.
2. The output is sent to an 8-bit ADC. Evaluate the output S/N ($4k_BT \approx 1.646 \times 10^{-20}$ J).
3. To improve S/N, the signal x is pulsed with on-time $T_p = 1$ ms and frequency of 1 Hz, and a boxcar averager is placed after the amplifier. Find the BA parameters granting $S/N = 10$.
4. Consider the case in which the current source $I_{ref} = 1$ mA is replaced by a voltage source $V_{ref} = 50$ mV. Would it be a convenient choice (provide explanations for your answer)?

Do a good job!

Results will be posted by January 28th **Mark registration: by February 1st**

Solution

Problem 1

1.1

The non-inverting input of the OA is at bias

$$V^+ = I_i R_1,$$

obviously equal to V^-. The KCL at the inverting node leads to

$$\frac{V_o - V^-}{R_2} = I_i + \frac{V^-}{R_1} = 2I_i \Rightarrow V_o = I_i R_1 + 2I_i R_2 = I_i(R_1 + 2R_2).$$

The transresistance gain of the stage is $R_1 + 2R_2 = 12.5$ MΩ.

1.2

Capacitor C_i will introduce a pole and no zero in the loop transfer, so we can compute the zero-frequency transfer first, and add the pole later. Removing the capacitor, we obtain

$$G_{loop} = -A(s)\frac{R_1}{R_1 + R_2},$$

while the resistance seen by the capacitor C_i is $R_c = R_1 + R_1 \parallel R_2 = 2.36$ MΩ, leading to the final result

$$G_{loop} = -A(s)\frac{R_1}{R_1 + R_2}\frac{1}{1 + sC_i R_c}.$$

The pole introduced by C_i is $f_p = 1/(2\pi R_c C_i) = 33.79$ kHz, where $|G_{loop}(f_p)| = G_{loop}(0) f_0/f_p \approx 11 \approx 21$ dB; the system is unstable, having $f_{0dB} = f_p\sqrt{11} \approx 112$ kHz and $\phi_m = 90 - \arctan(f_{0dB}/f_p) \approx 17°$.
One possible compensation scheme is the usual one that involves placing a capacitor C_c in parallel to R_2 (Fig. 1, left). We know that such a configuration places a zero with a time constant equal to $R_2 C_c$, but we will just carry out the full calculation: Labelling $Z_1 = R_1 \parallel (R_1 + 1/sC_i) = R_1(1 + sC_i R_1)/(1 + 2sC_i R_1)$ and $Z_2 = R_2/(1 + sC_c R_2)$, we get, after some manipulation

$$G_{loop} = -A(s)\frac{Z_1}{Z_1 + Z_2}\frac{1}{1 + sC_i R_1} = -A(s)\frac{R_1}{R_1 + R_2}\frac{1 + sC_c R_2}{1 + s(C_i R_c + C_c R_p) + s^2 C_i C_c R_1 R_p},$$

where $R_p = R_1 \parallel R_2$. We can now set C_c by placing the zero at f_{0dB}, i.e., $C_c = 1/(2\pi f_{0dB} R_2) \approx 0.25$ pF. The new (approximated) pole position is

$$f_p \approx \frac{1}{2\pi(C_i R_c + C_c R_p)} = 32 \text{ kHz},$$

where $|G_{loop}(f_p)| = 11.78$, $f_{0dB} \approx 110$ kHz and $\phi_m = 90 - \arctan(f_{0dB}/f_p) + \arctan(f_{0dB}/f_z) \approx 61°$. The HF pole is around 1.2 MHz. The resulting loop gain is shown in Fig. 1 (right) and the exact value of ϕ_m is 63.3°.

1.3

If we consider for simplicity the original scheme, we see that the voltage noise is amplified by the non-inverting gain $(R_1 + R_2)/R_1$, meaning that

$$\sqrt{\overline{V_o^2}} = \sqrt{S_V \left(\frac{R_1 + R_2}{R_1}\right)^2 \frac{\pi}{2} f_{0dB}} \approx 22\ \mu\text{V}.$$

Just as a reference, considering the compensated circuit we get (no current flows in C_i)

$$V_o = V_n\frac{R_1 + Z_2}{R_1} = V_n\frac{R_1 + R_2}{R_1}\frac{1 + sC_c R_p}{1 + sC_c R_2}.$$

Note that the pole is at the same frequency as f_{0dB}, so in this case we obtain the same previous result (a small correction should be placed, as there are now two poles rather than one).

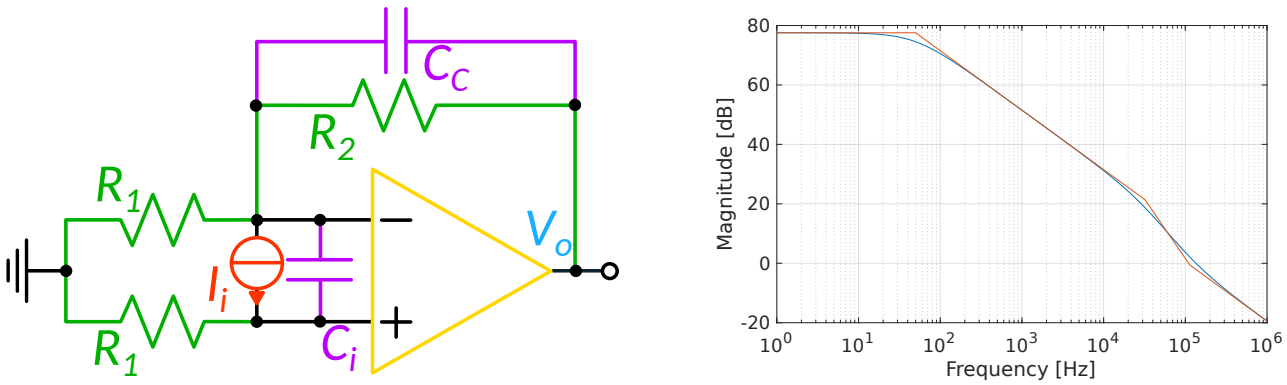


Figure 1: Left = Compensated scheme. Right = Resulting loop gain.

1.4

When there is no signal applied, the output must lay at $V_{cc}/2$ to maximize the output voltage range. The input pins should also be at the same voltage, to avoid unnecessary DC current flow and power consumption. One possibility could be to replace the lower R_1 resistor with a voltage divider made up of two equal $2R_1$ resistors, placing then a DC-blocking capacitor in series to the other R_1 resistor, as depicted in Fig. 2 (left). Another solution could be to directly replace the ground node at the left with a $V_{cc}/2$ bias, obtained via a voltage divider from V_{cc}. This has the advantage of not requiring a capacitor, but the divider resitances will change the gain! To keep this change small, such resistors must be much lower than R_1, R_2, meaning that a significant current is drawn and wasted.
In reality the solution could be more complex, mainly dependent on the nature of the signal (for example, if I_i comes from a photodiode, a DC bias across it is also needed).

Problem 2

2.1

We can apply the superposition principle, noting that the value of the input bias does not result in any current. Setting it to zero, we then obtain

$$\begin{aligned} I_1 &= I_{ref}\frac{R_2}{R_1+R_2} = I_{ref}\frac{1-x}{2} \\ I_2 &= I_{ref}\frac{R_1}{R_1+R_2} = I_{ref}\frac{1+x}{2} \end{aligned} \Rightarrow V_o = G(I_2-I_1) = GI_{ref}x.$$

We then obtain $G = V_o^{max}/(I_{ref}x_{max}) = 5/(10^{-3}10^{-1}) = 50$ kΩ.

2.2

The scheme for evaluating the input noise current of the amplifier can be drawn as in Fig. 2 (right), from which we can obtain (remember that PSD transfer functions must be separately squared)

$$\begin{aligned} I_1 &= I^- + \frac{V_n}{2R} + \frac{V_{R_1}}{2R} + \frac{V_{R_2}}{2R} \\ I_2 &= I^+ - \frac{V_n}{2R} - \frac{V_{R_1}}{2R} - \frac{V_{R_2}}{2R} \end{aligned} \Rightarrow S_{V_o} = G^2 S'_{V_o} = G^2(2S_I + 2S_R + S_V/R^2) \approx 10^{-16}G^2 \quad [\mathrm{V}^2/\mathrm{Hz}],$$

where $S_R = 4k_BT/R$. The minimum signal is $V_o^{max}/2^8$, leading to

$$\left(\frac{S}{N}\right) = \frac{V_o^{max}}{2^8\sqrt{S_{V_o}}} \approx \frac{I_{ref}x_{max}}{2^8\sqrt{S'_{V_o}(\pi/2)f_p}} \approx 0.3.$$

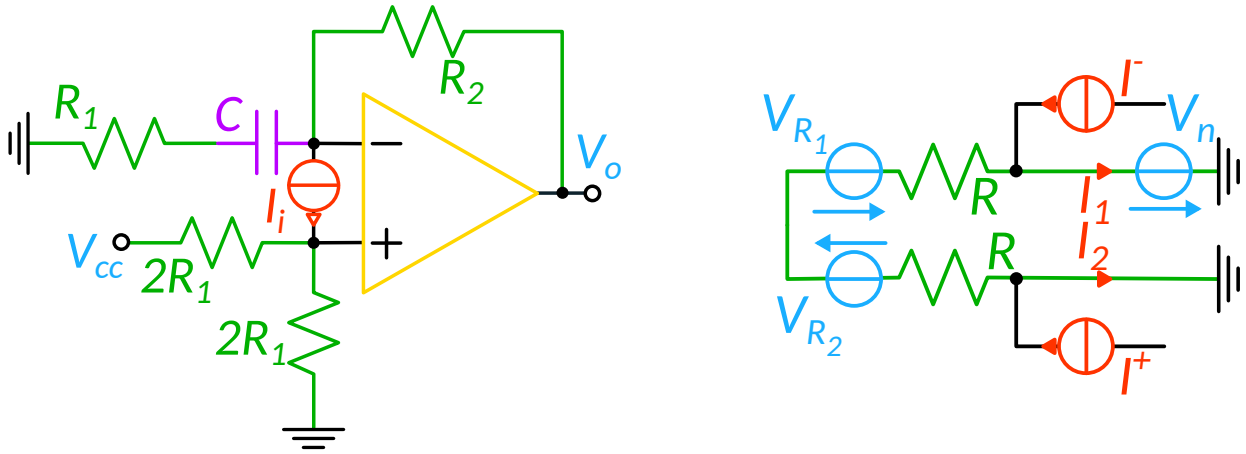


Figure 2: Left = Scheme suitable for single-supply operation. Right = Current-mode bridge scheme for noise calculations.

2.3

The easiest solution is to remember that a BA stage has the same S/N of an LPF with time constant T_F, meaning that we can simply replace f_p with $f_{BA} = 1/(2\pi T_F)$ in the above equation, obtaining:

$$\left(\frac{S}{N}\right)_{BA} = \frac{I_{ref} x_{max}}{2^8 \sqrt{S'_{V_o}(\pi/2) f_{BA}}} = 10 \Rightarrow f_{BA} \approx 9.7 \text{ Hz}.$$

This means $T_F = 1/(2\pi f_{BA}) = 16.4$ ms and $N_{eq} = 2T_F/T_P \approx 33$.

2.4

For the voltage source case, the output of the amplifier would be

$$V_o = G\left(\frac{V_{ref}}{R(1-x)} - \frac{V_{ref}}{R(1+x)}\right) = G\frac{2V_{ref}}{R}\frac{x}{1-x^2},$$

to be compared with the result in #2.1. Since $2V_{ref}/R = I_{ref}$, the two outputs look very similar, but there is a couple of disadvantages in this solution: First, the term at the denominator adds a non-linearity. This is indeed a small error, equal to 1% for the case of $x = 0.1$ and it might be negligible. The second and way more undesirable point is the dependence on R, meaning that any change in resistor value (due to temperature, aging,...) will affect the output.