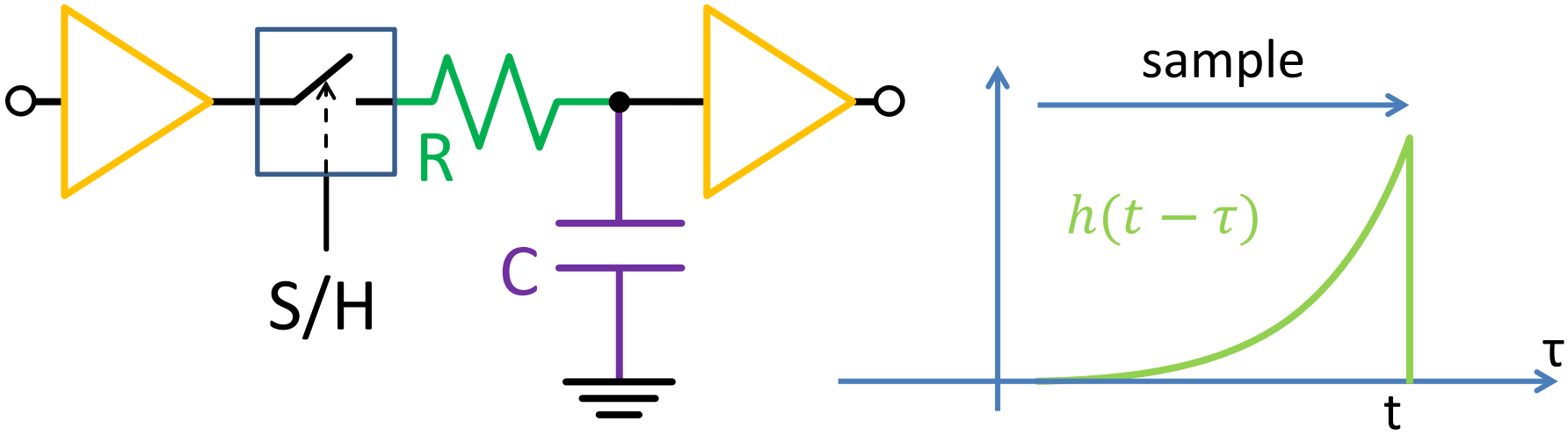
Sample & hold amplifiers
ADC parameters

Alessandro Spinelli
Tel. (02 2399) 4001
alessandro.spinelli@polimi.it
home.deib.polimi.it/spinelli

Slides are supplementary material and are NOT a replacement for textbooks and/or lecture notes

Sample & hold amplifiers (SHAs)

Basic SHA scheme



- R is the resistance of the non-ideal switch
- In the ideal case, $h(t-\tau) = \delta(t-\tau)$

Output S/N

- The output noise is

$$\overline{n_{RC}^2} = 4k_B T R \frac{1}{4RC} = \frac{k_B T}{C}$$

- A gate time $T_G \ll RC$ could be used for fast sampling (gated integrator). The output noise (for unity signal gain) would be

$$\overline{n_{GI}^2} = 4k_B T R \frac{1}{2T_G} \gg \overline{n_{RC}^2}$$

Parameters

From [1]

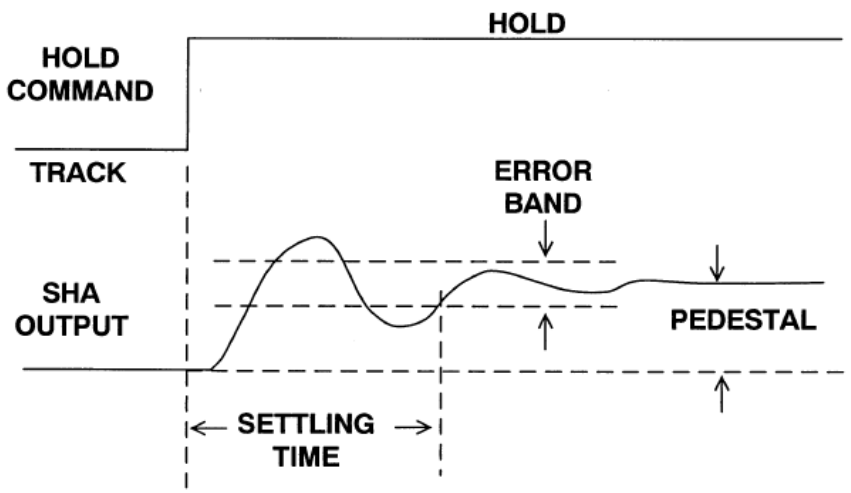
SAMPLE MODE	SAMPLE-TO-HOLD TRANSITION	HOLD MODE	HOLD-TO-SAMPLE TRANSITION
STATIC: ◆ Offset ◆ Gain Error ◆ Nonlinearity	STATIC: ◆ Pedestal ◆ Pedestal Nonlinearity	STATIC: ◆ Droop ◆ Dielectric Absorption	
DYNAMIC: ◆ Settling Time ◆ Bandwidth ◆ Slew Rate ◆ Distortion ◆ Noise	DYNAMIC: ◆ Aperture Delay Time ◆ Aperture Jitter ◆ Switching Transient ◆ Settling Time	DYNAMIC: ◆ Feedthrough ◆ Distortion ◆ Noise	DYNAMIC: ◆ Acquisition Time ◆ Switching Transient

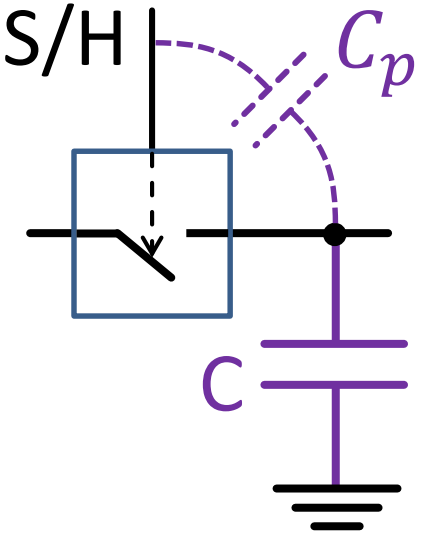
Here SHA behaves as an amplifier/follower

$\Rightarrow$ parameters are similar

Pedestal or Hold step

From [1]



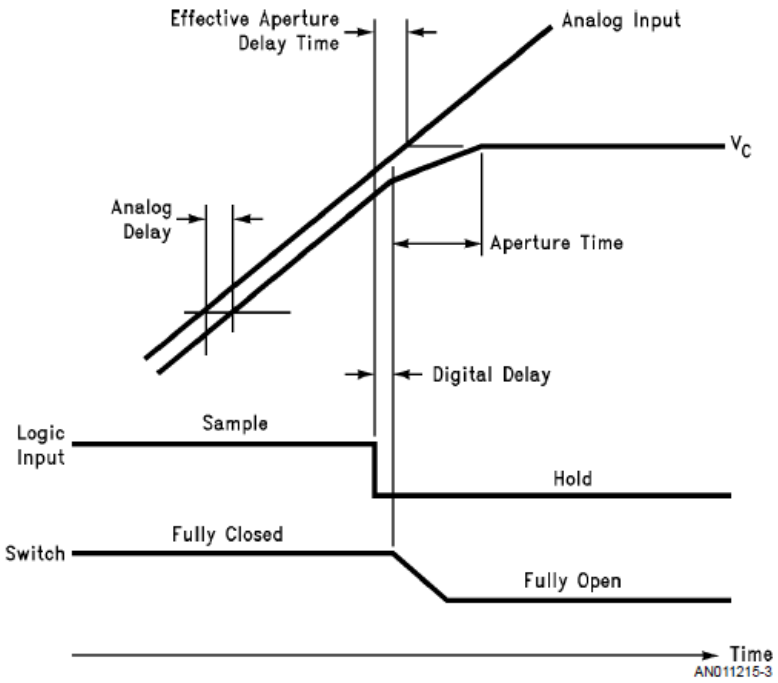


The error is due to parasitic injection through the non-ideal switch

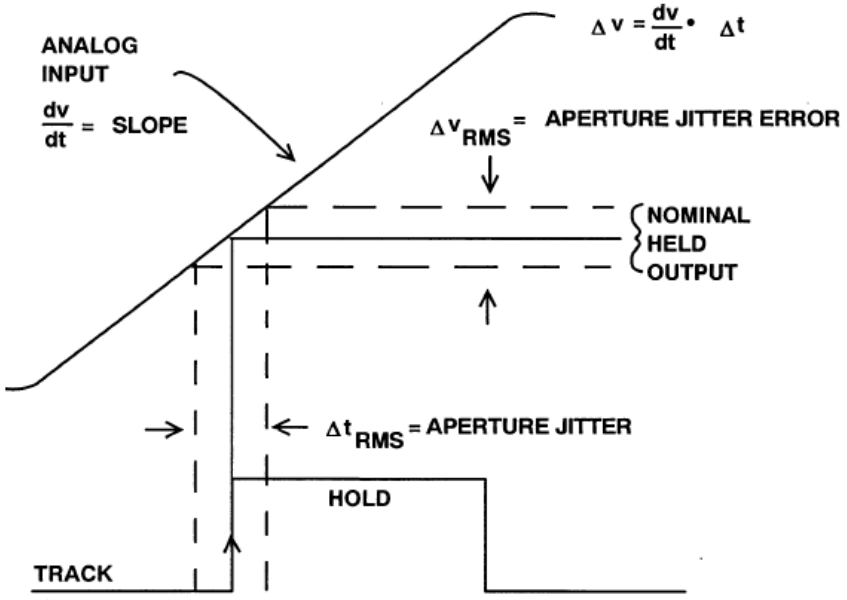
$$\Delta V \approx \Delta V_{S/H} \frac{C_p}{C_p + C}$$

Aperture time and jitter

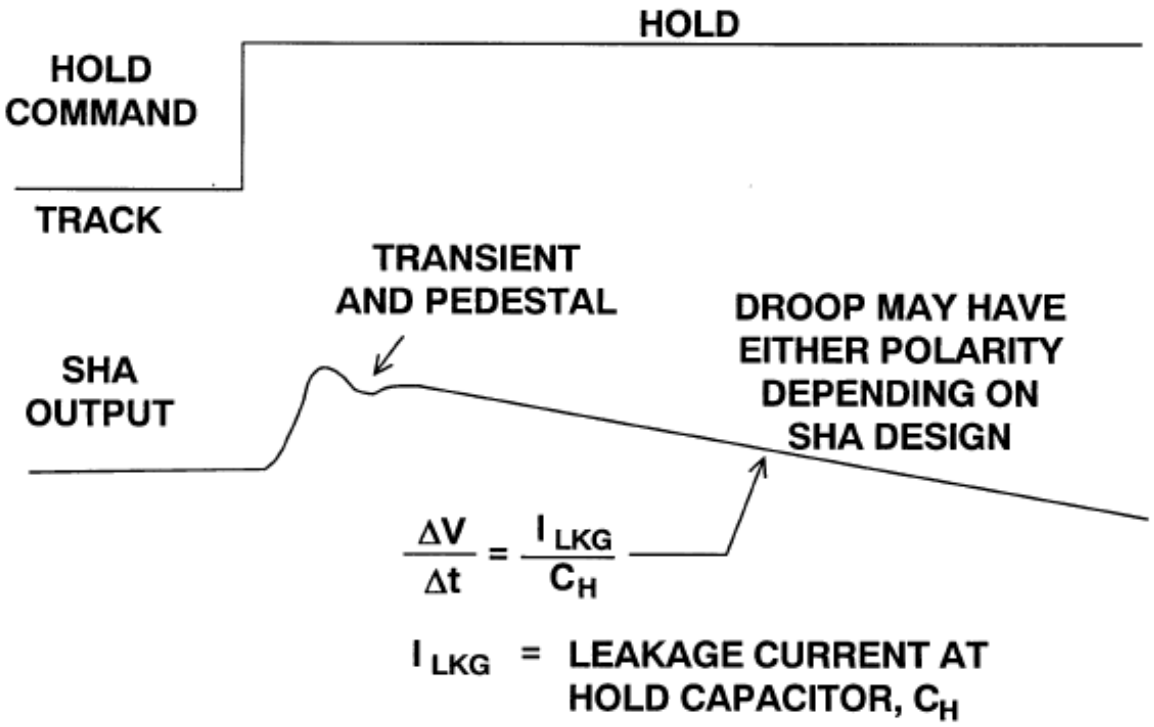
From [2]



From [1]



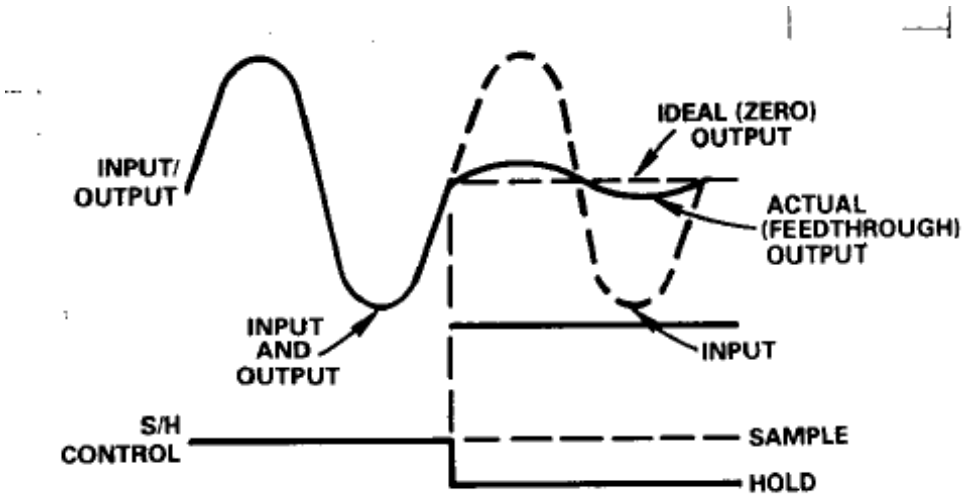
Droop rate

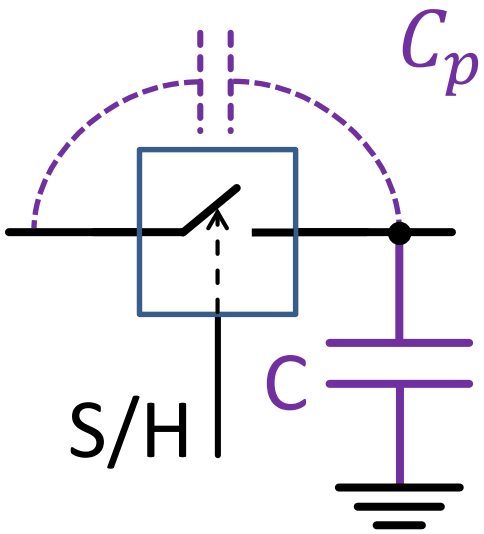


From [1]

Input feedthrough

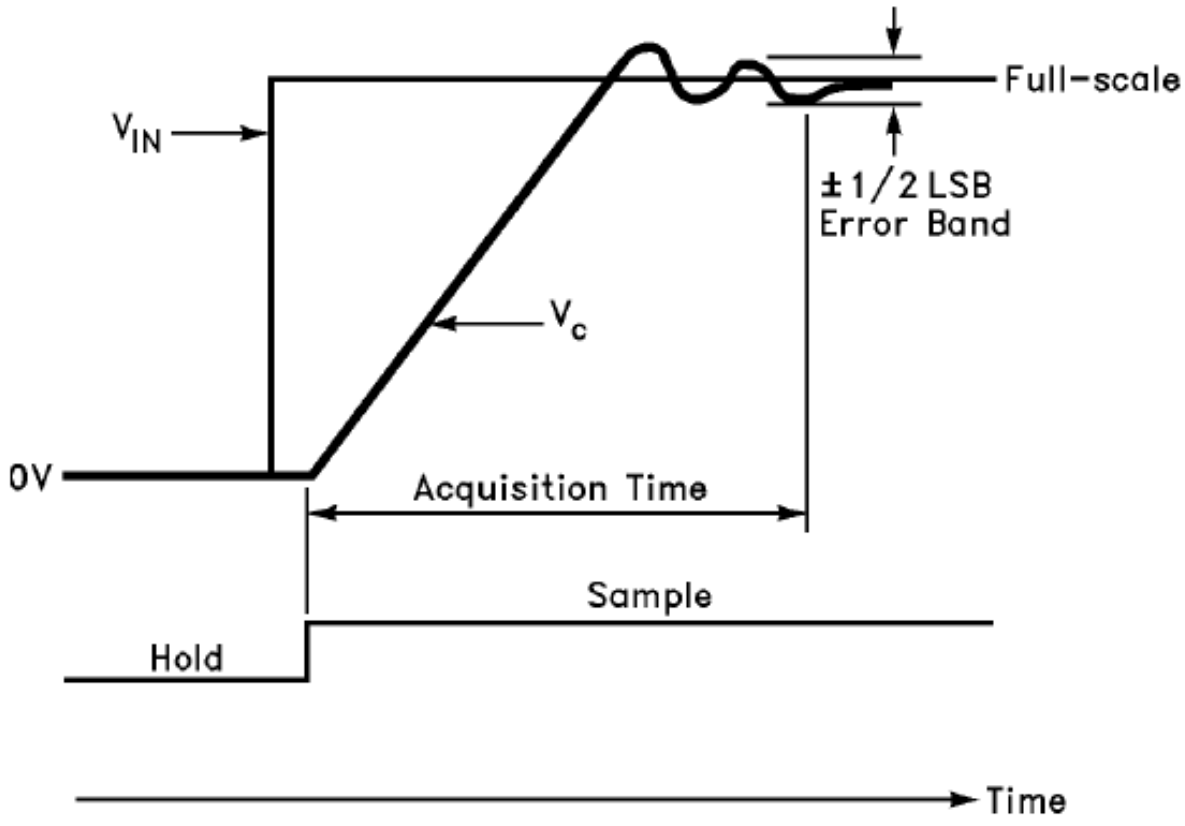
From [3]





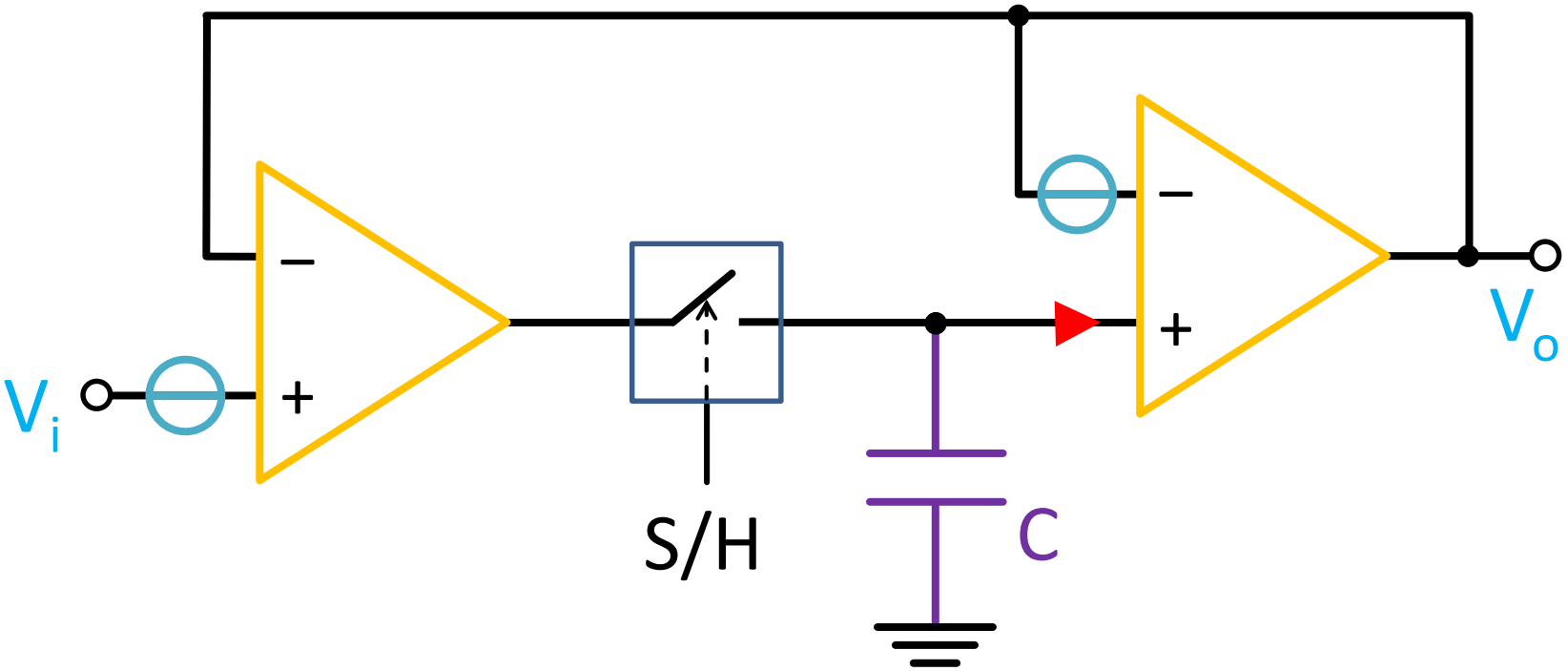
- Similar to hold step, $\Delta V \approx V_i C_p/(C_p + C)$
- C_p can be due to the switch as well as to parasitic layout coupling,…

Acquisition time



From [2]

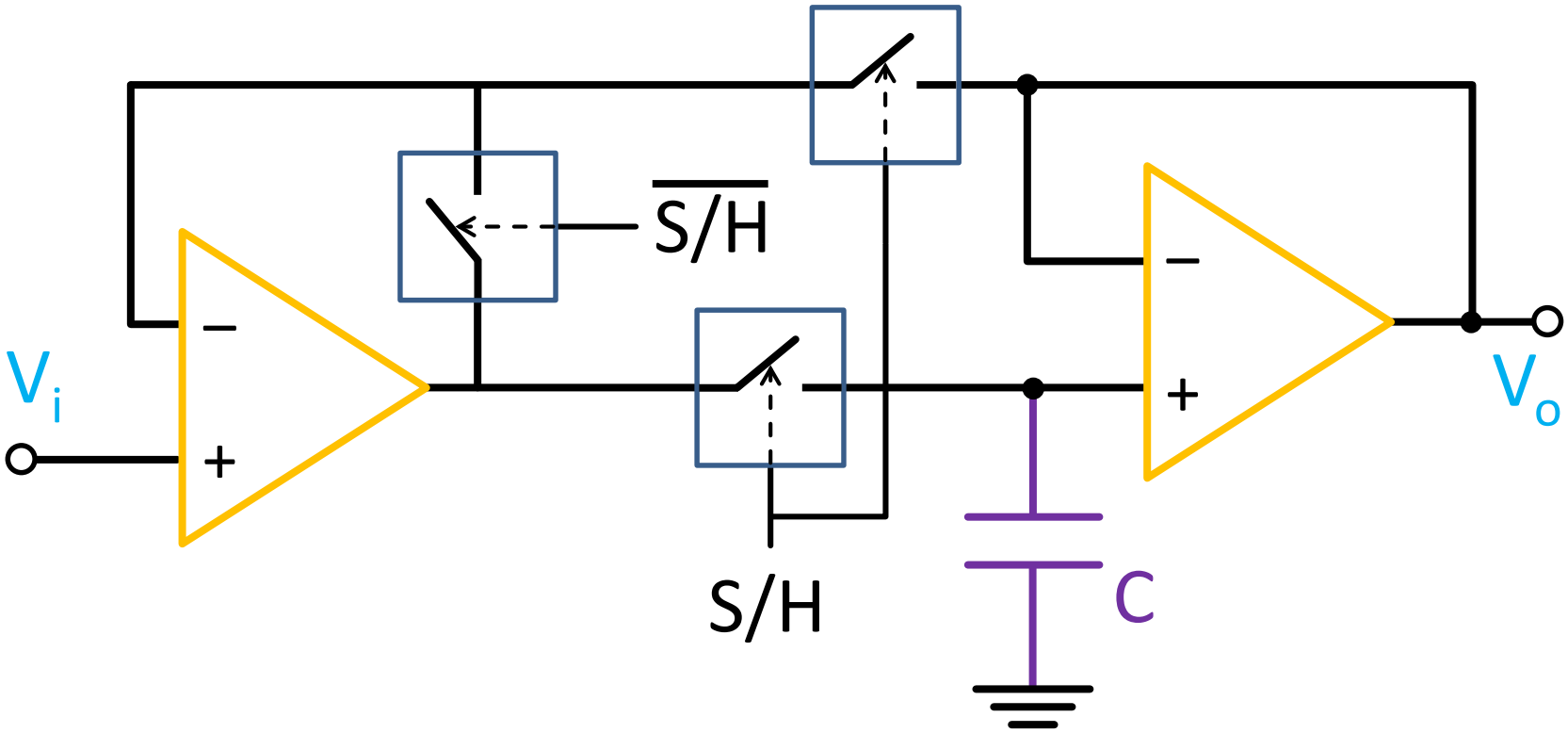
Improved scheme



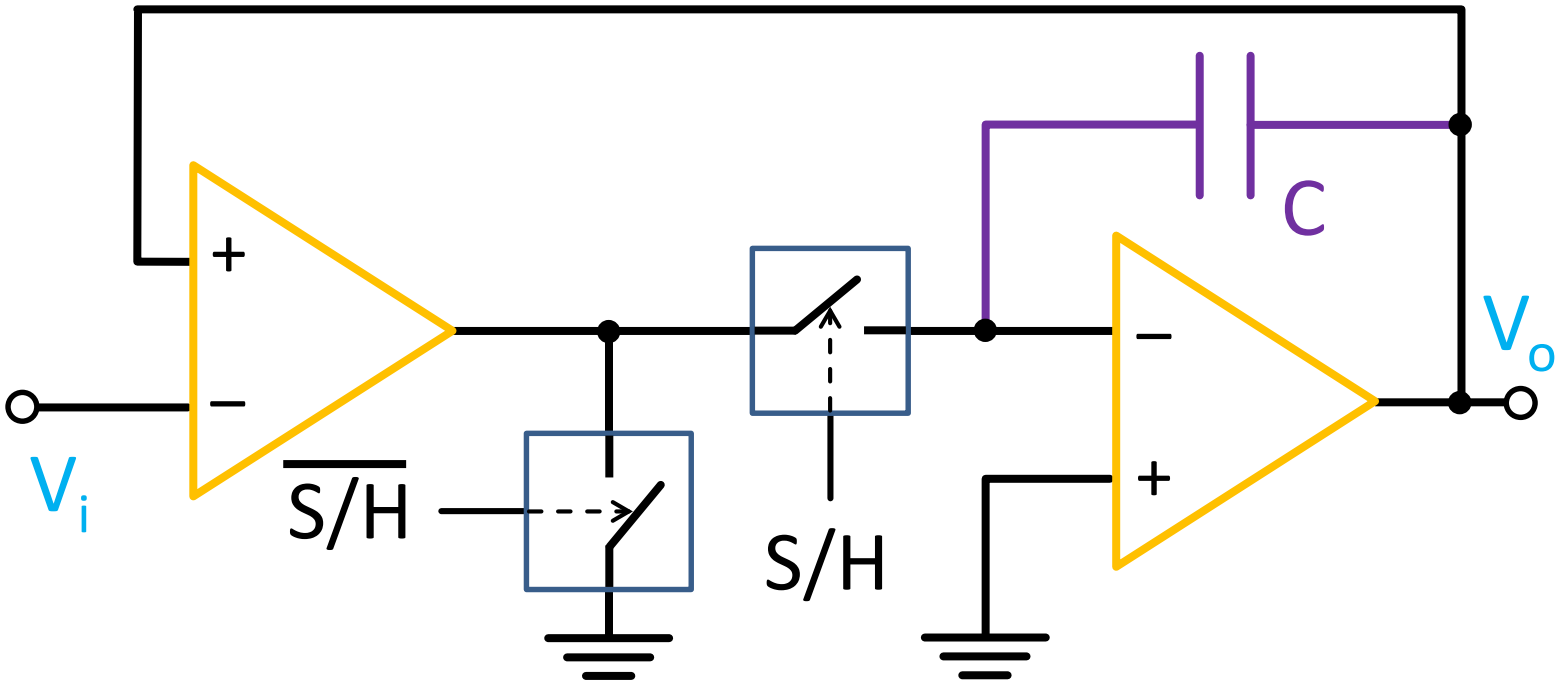
Pros and Cons

- Advantages
  - Impedance decoupling
  - Insensitive to V_{OS2}
- Limitations
  - Limited bandwidth owing to the stability requirement when the loop is closed
  - Saturation of the first OPAMP in Hold mode $\Rightarrow$ long acquisition time

Prevention of saturation



SHA with integrator

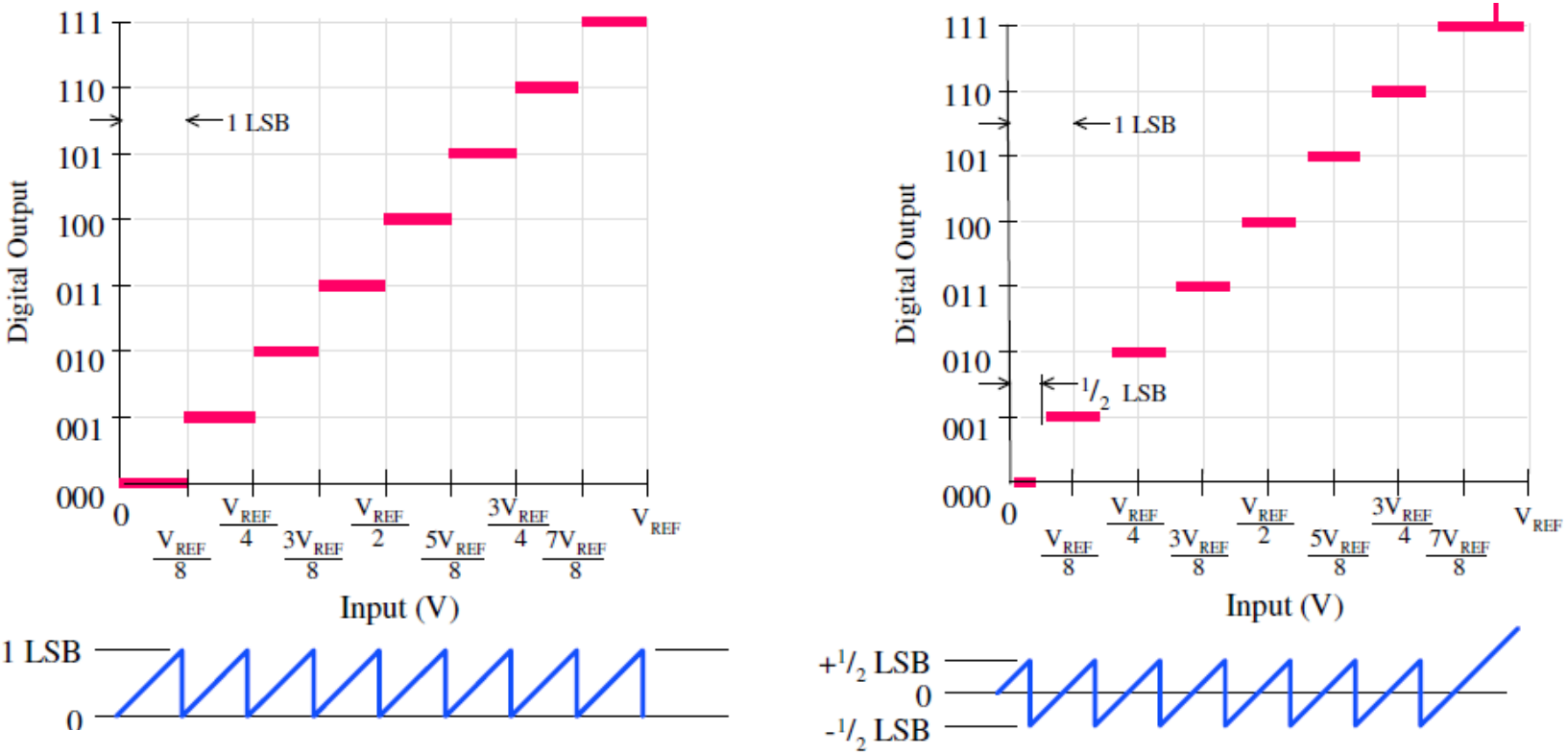


Pros and Cons

- Advantages
  - The S/H switch operates always near zero bias
    - Pedestal error is not input-dependent
    - Input feedthrough during Hold mode is reduced
- Limitations
  - Limited bandwidth owing to the stability requirement when the loop is closed
- Differential architectures with complementary switches can be used to improve performance

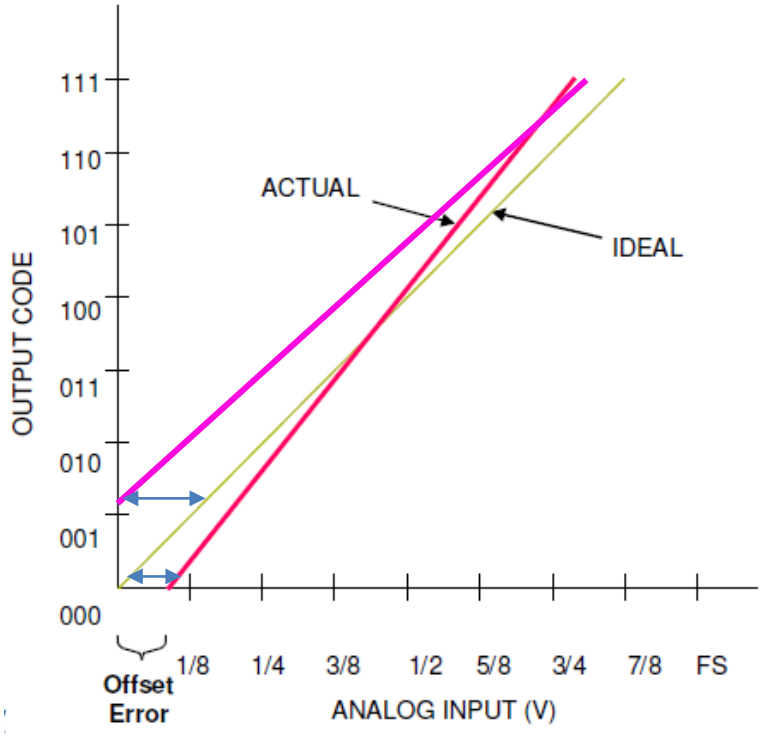
ADC DC Parameters

Quantization error



From [4]

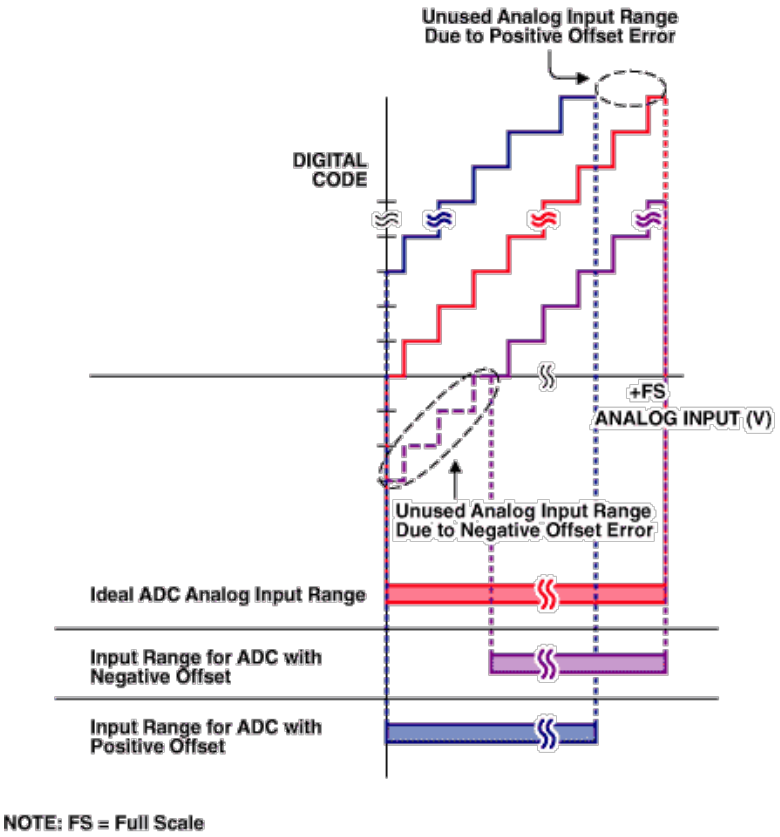
Offset error



Modified from [4]

Offset or Zero-scale error is the difference between actual and ideal first transition voltage

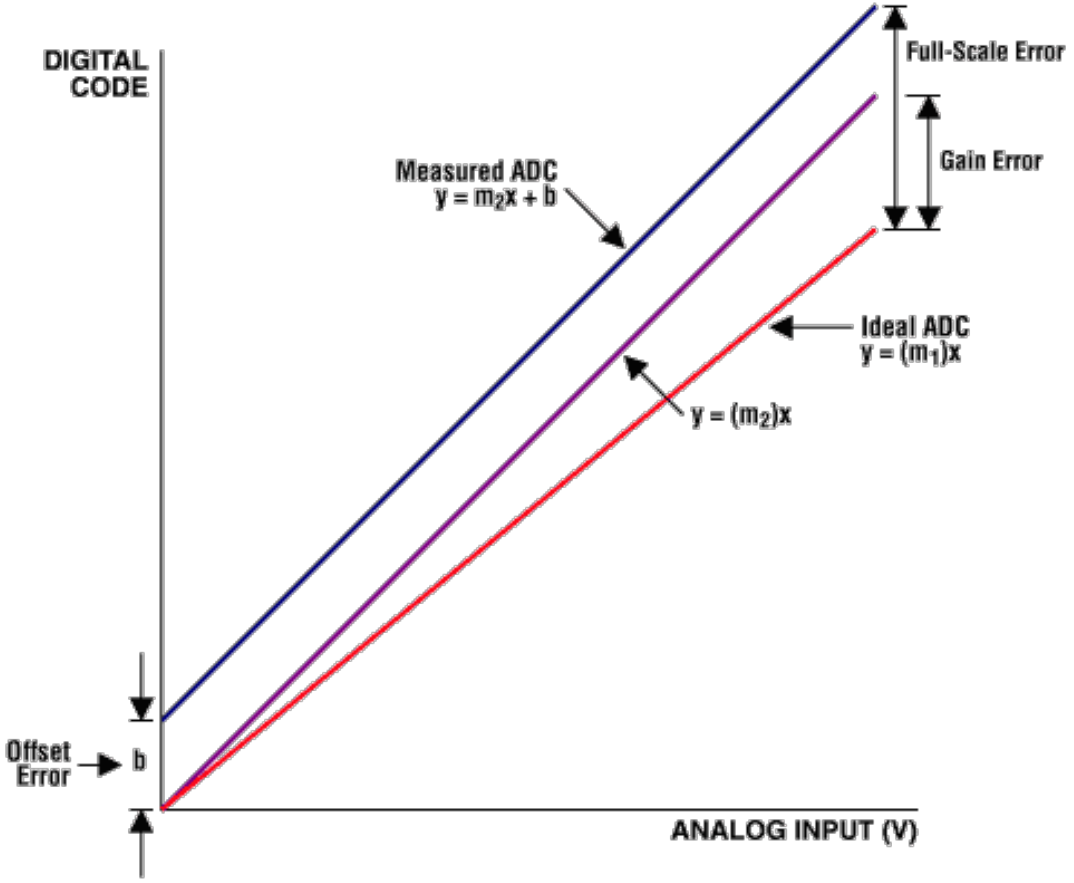
Offset and dynamic range



From [5]

Offset leads to a loss in the input range, i.e., a smaller dynamic range

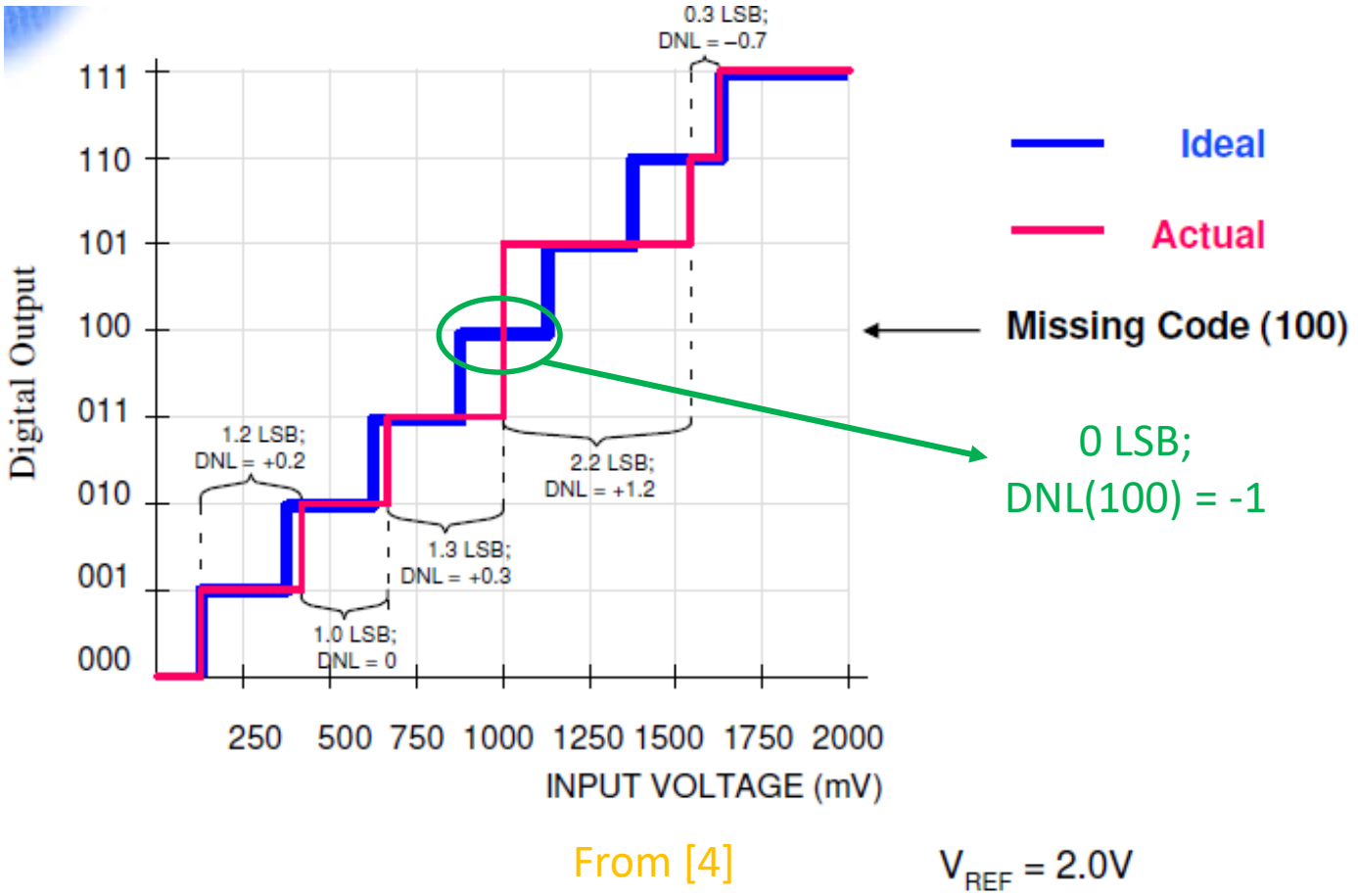
Gain and FS errors



DNL

- In an ideal ADC, the transitions are 1 LSB apart
- The difference between the actual and the ideal code width is called DNL
- DNL is measured for each input range or output code; however, only the maximum absolute value is reported

DNL and missing codes



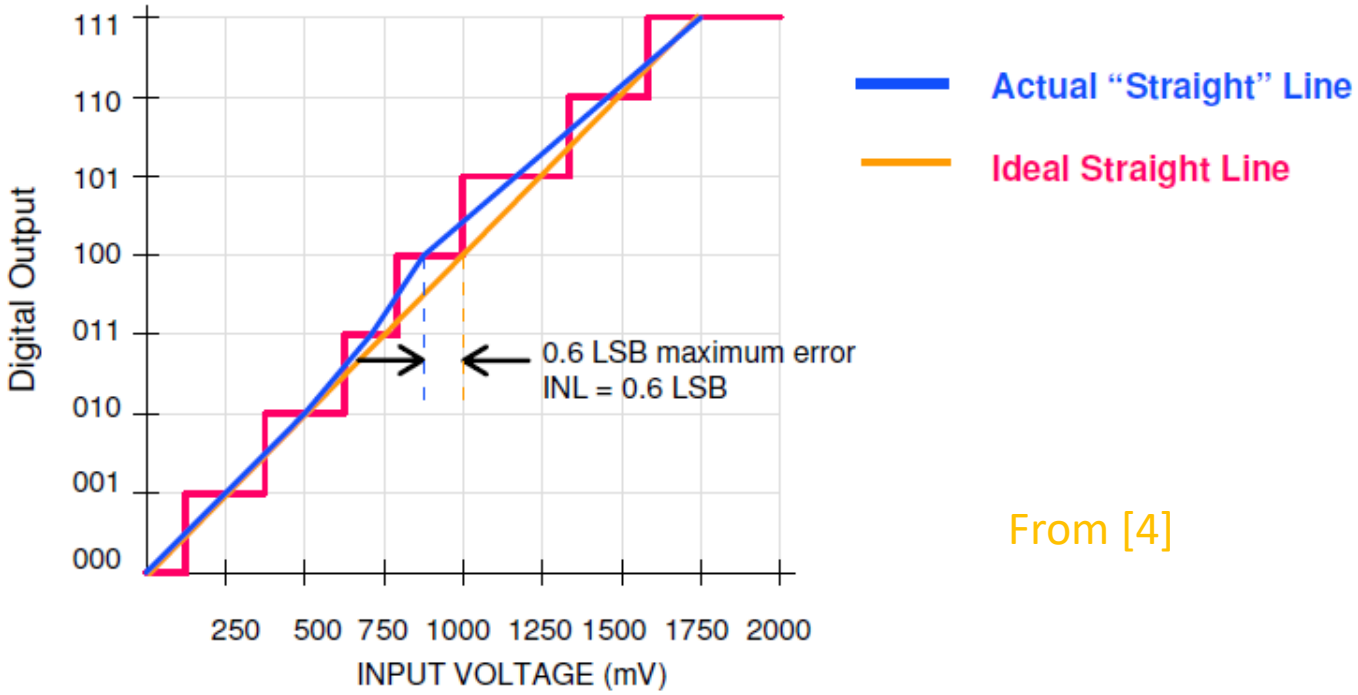
From [4]

V_{REF} = 2.0V

Remarks

- If DNL is defined for each output code (see [6]), obviously DNL = -1 $\Rightarrow$ missing code!
- If DNL is defined for each input range (see [4]), it is aways > -1. DNL ≥ 1 does not imply the existence of missing codes
- The manufacturer usually specifies if the ADC has missing codes
- If $|DNL| < 1 \Rightarrow$ ADC is monotonic

INL

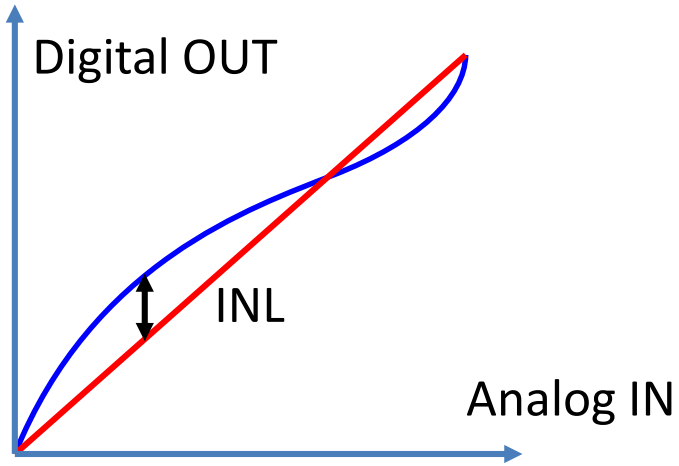


From [4]

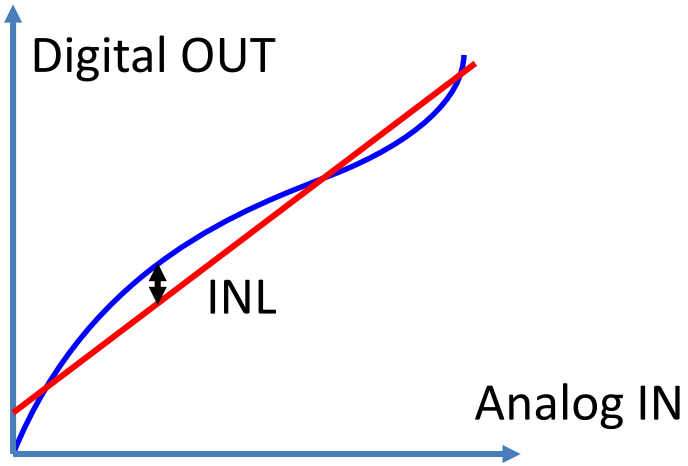
- INL is the maximum difference between the real characteristic and an ideal linear behavior
- INL is the sum of DNL errors

Which straight line?

End-points INL



Best-fit INL



- Offset and gain errors are first removed
- End-point INL is easier and most practical
- Best-fit INL gives lower values but is impractical in most applications

Other parameters…

- Code-edge noise
- Output noise
- Voltage reference specs
  - T drift
  - Voltage noise
  - Long-term stability
  - Load regulation
  - …

ADC AC Parameters

SNR

- Maximum amplitude of sinusoid is $A = V_{ref}/2$
- Signal power

$$\langle V_o^2 \rangle = \langle A^2 \sin^2 \omega t \rangle = \frac{A^2}{2} = \frac{V_{ref}^2}{8} = \frac{2^{2n}\Delta^2}{8}$$

- Noise power = quantization noise $\Delta^2/12$

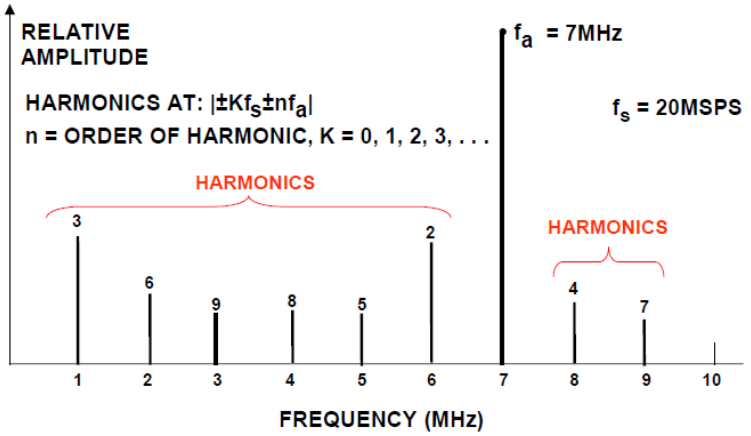
$$SNR^2 = \frac{2^{2n}\Delta^2}{8}\frac{12}{\Delta^2} = \frac{3}{2}2^{2n}$$

$$SNR_{dB} = 10\log_{10}\left(\frac{3}{2}2^{2n}\right) = 6.02n + 1.76$$

SINAD

- If additional noise is present, SNR decreases with respect to the ideal value
- Another component is (harmonic) distorsion

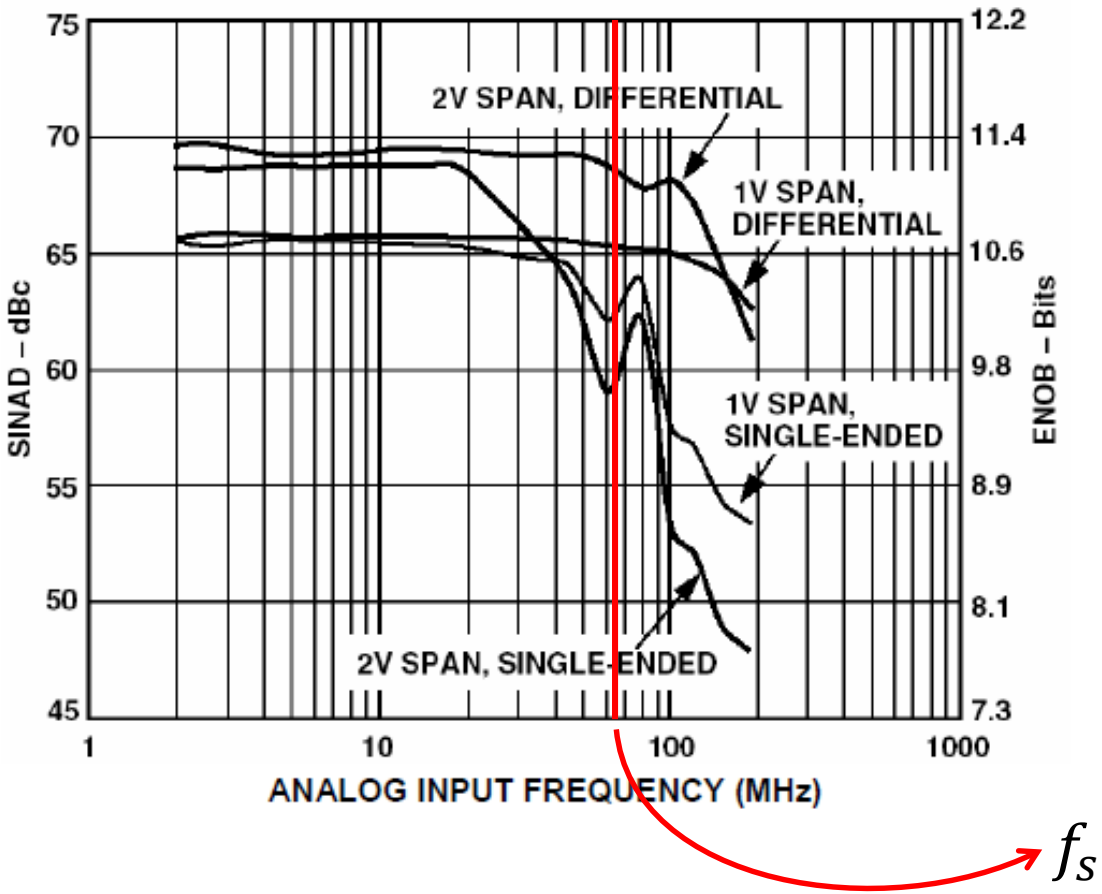
From [7]



$$SINAD = \frac{\text{rms signal}}{\text{rms (noise + distorsion)}} < \text{SNR}$$

SINAD vs. frequency

From [7]



ENOB

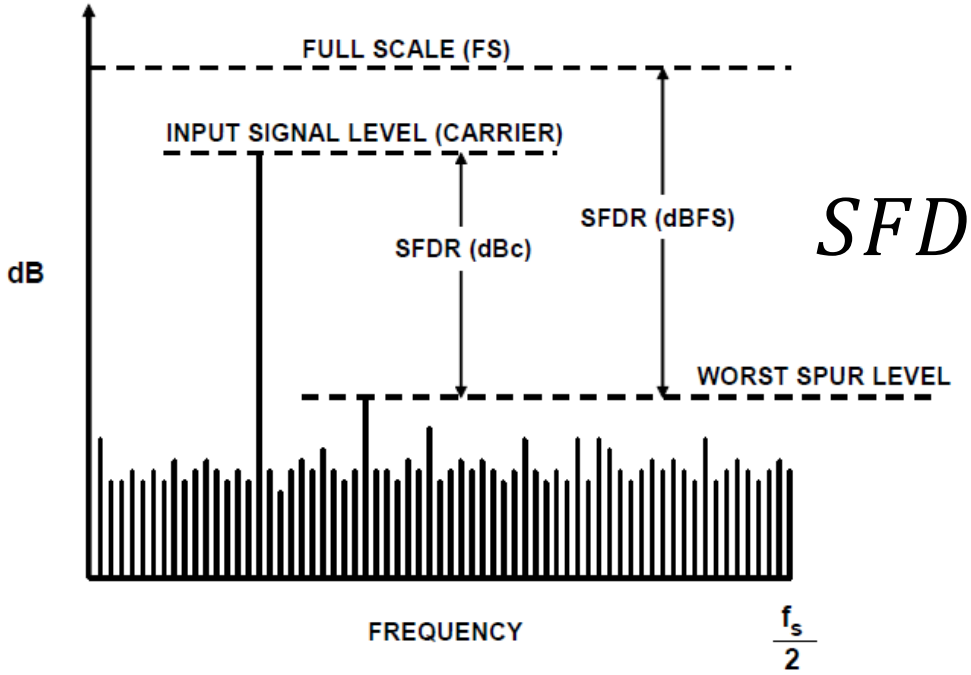
- SINAD is expressed as an effective number of bits (ENOB) via the SNR formula

$$ENOB = \frac{SINAD_{dB} - 1.76}{6.02} < n$$

- Don't confuse ENOB with resolution bits

SFDR

From [7]



$$SFDR = \frac{\text{rms signal}}{\text{rms worst spur}}$$

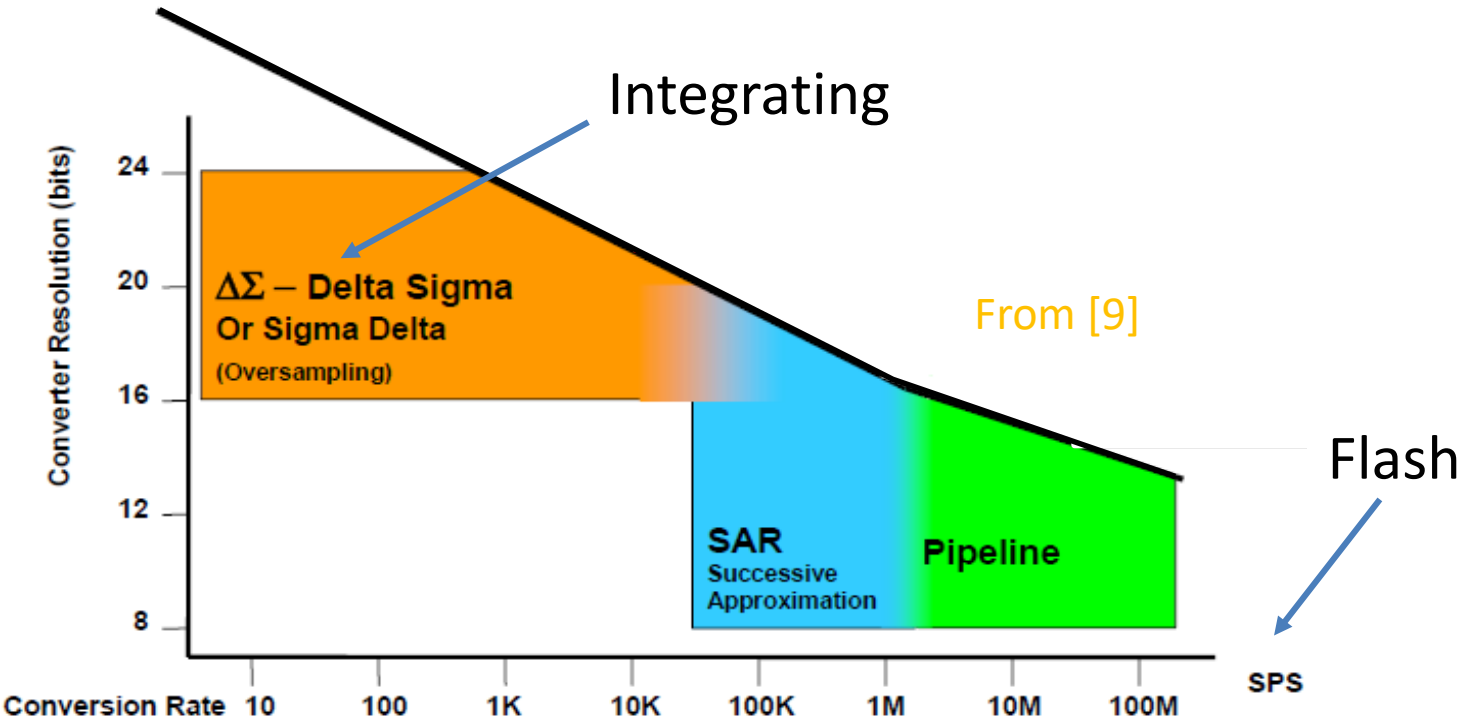
SFDR represents the smallest signal that can be distinguished from a large interference

ADC technologies

From [8]

	FLASH (Parallel)	PIPELINE	SAR	SIGMA DELTA	DUAL SLOPE (Integrating)
Pick This Architecture if you want:	Ultra-high speed when power consumption not a primary concern	High speeds, few Msps to 100+ Msps, 8 bits to 16 bits, lower power consumption than flash	Medium to high resolution (8 to 16bit), 5Msps and under, low power, small size	High resolution, low to medium speed, no precision external components, simultaneous 50/60Hz rejection, digital filter reduces anti-aliasing requirements	Monitoring DC signals, high resolution, low power consumption, good noise performance
Conversion Method	N bits – 2^N - 1 comparators caps increase by a factor of 2 for each bit	Small parallel structure, each stage works on one to a few bits	Binary search algorithm, internal circuitry runs higher speed	Oversampling ADC, 5-Hz – 60 Hz rejection programmable data output	Unknown input voltage is integrated and value compared against known reference value
Disadvantages	Sparkle codes / metastability, high power consumption, large size, expensive	Parallelism increases throughput at the expense of power and latency	Speed limited to ~5Msps. May require anti-aliasing filter	Higher order (4th order or higher) - multibit ADC and multibit feedback DAC	Slow conversion rate. High precision external components required to achieve accuracy
Conversion Time	Does not change with increased resolution	Increases linearly with increased resolution	Increases linearly with increased resolution	Tradeoff between data output rate and noise free resolution	Doubles with every bit increase in resolution
Component Matching Requirements	Typically limits resolution to 8 bits	Double with every bit increase in resolution	Double with every bit increase in resolution	Double with every bit increase in resolution	Does not increase with increase in resolution
Size	2^N-1 comparators, Die size and power increases exponentially with resolution	Die increases linearly with increase in resolution	Die increases linearly with increase in resolution	Core die size will not materially change with increase in resolution	Core die size will not materially change with increase in resolution

Resolution and conversion rate



Final choice will depend on application (see discussion in [9])

References

1. http://www.analog.com/static/imported-files/tutorials/MT-090.pdf
2. http://www.ti.com/lit/an/snoa223/snoa223.pdf
3. http://www.analog.com/static/imported-files/application_notes/488661392773185976219800 6746AN270.pdf
4. http://www.unirioja.es/cu/lzorzano/ABCs_of_ADCs.pdf
5. http://www.maximintegrated.com/app-notes/index.mvp/id/748
6. http://www.freescale.com/files/microcontrollers/doc/app_note/AN2438.pdf
7. http://www.analog.com/static/imported-files/tutorials/MT-003.pdf
8. http://www.maximintegrated.com/app-notes/index.mvp/id/2094
9. http://www.ti.com/europe/downloads/Choose%20the%20right%20data%20converter%20for%20your%20application.pdf