POLITECNICO DI MILANO

Electronics – 96032





OpAmps Offset Voltage and Bias Currents

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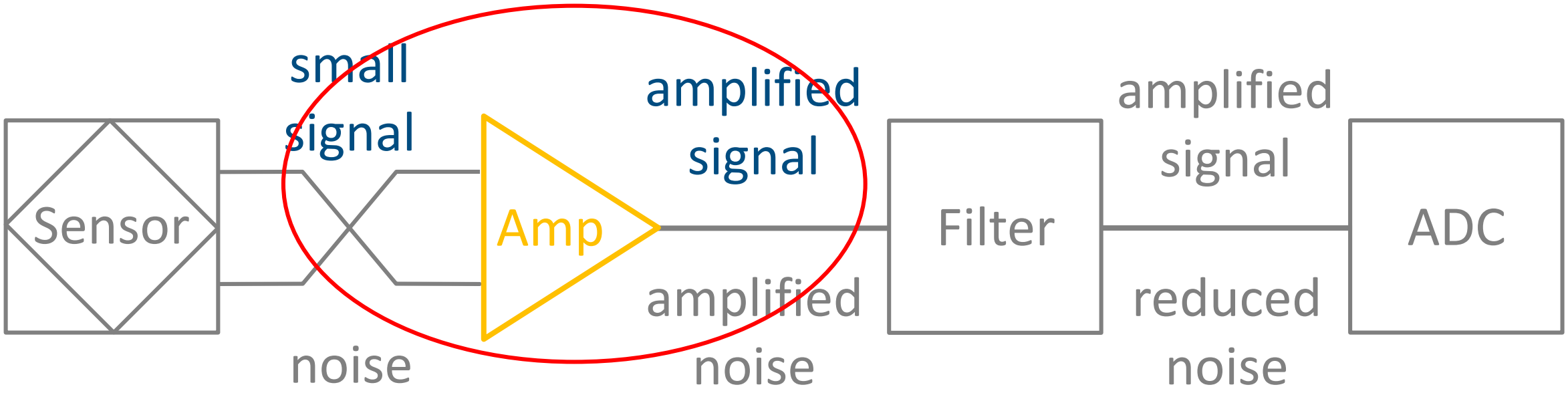
Disclaimer

Slides are supplementary material and are NOT a replacement for textbooks and/or lecture notes

Acquisition chain



next lessons

Purpose of the lesson

- We begin our study with the analysis and design of simple amplifiers
- Next lessons will deal with
  - Basic amplifier principles and the feedback amplifier concept
  - Linear applications of OpAmps (this lesson)
  - Feedback amplifier properties
  - Stability of feedback amplifiers
  - Instrumentation amplifiers and OpAmp parameters

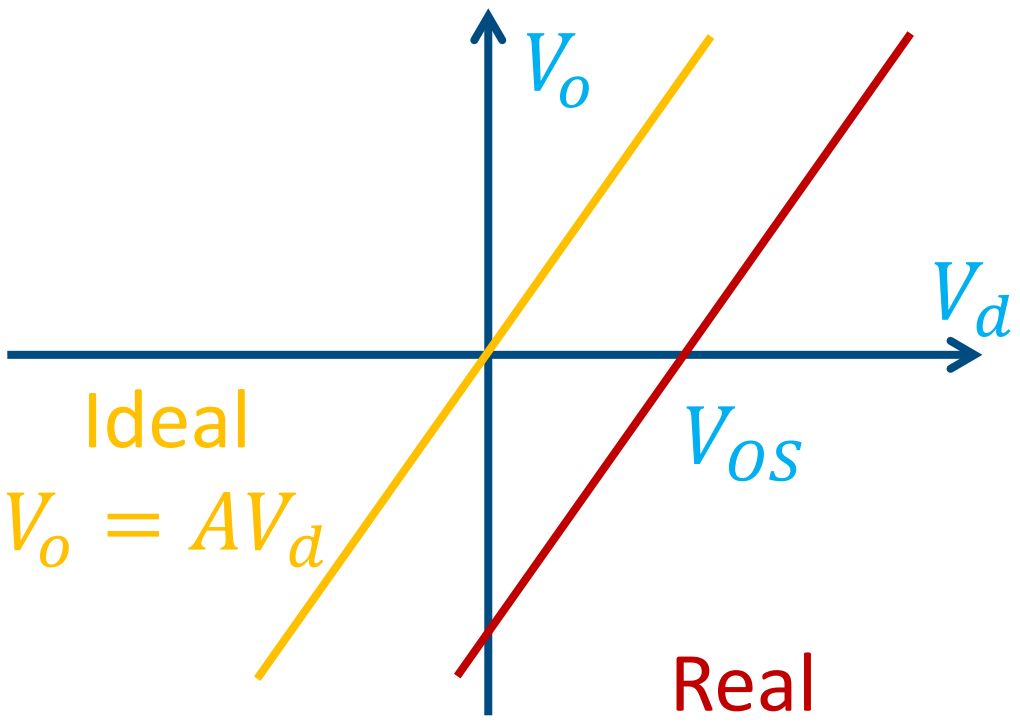
Outline

- Offset voltage
- Bias currents
- Effect on linear circuits

OA parameters

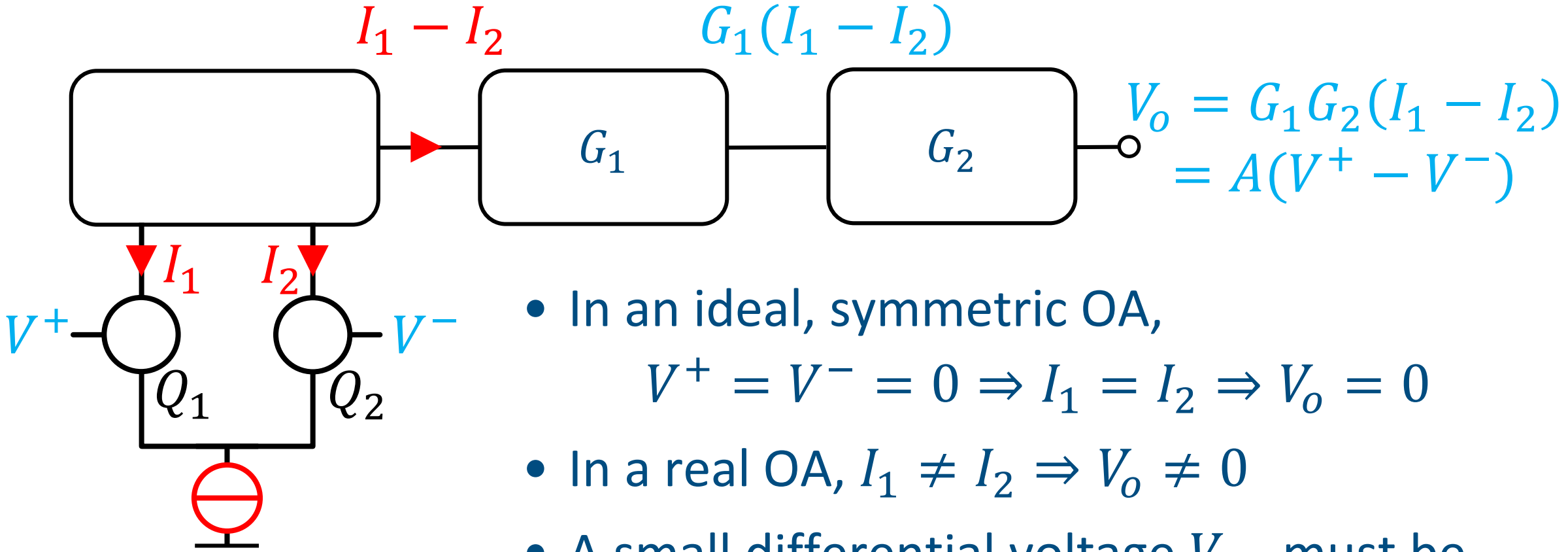
- We begin to remove the OA ideality assumption and discuss the impact on circuits
- OA properties are described by appropriate parameters detailed in manufacturers' datasheets
- There are many OA to choose from
  - Different technology (BJT, JFET, CMOS)
  - Different types (precision, low-drift, rail-to-rail,…)

Input offset voltage



- In an ideal OA, $V_d = 0 \Rightarrow V_o = 0$
- In real OA, $V_d = 0 \Rightarrow V_o \neq 0$
- The offset voltage is the value of V_d that must be applied to bring the output to zero
- Typ. 1-5 mV (absolute value is always specified)
- Precision OAs have $V_{OS} < 1$ mV

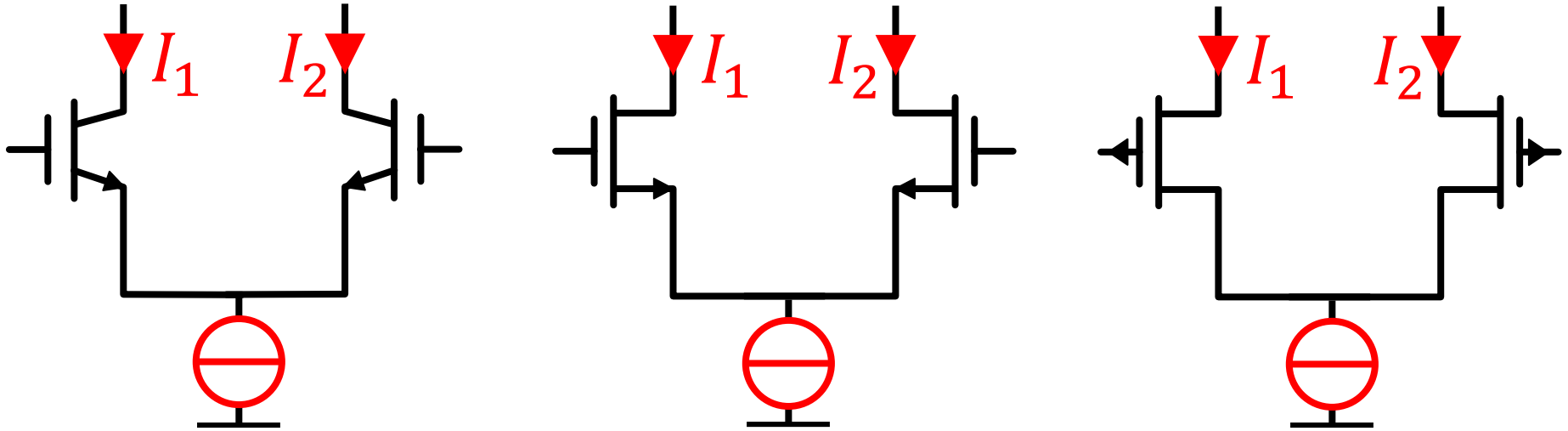
Origin of offset voltage



$$V_{OS} \propto \frac{\Delta I}{g_m}\left(+\Delta V_{T/P}\right)$$

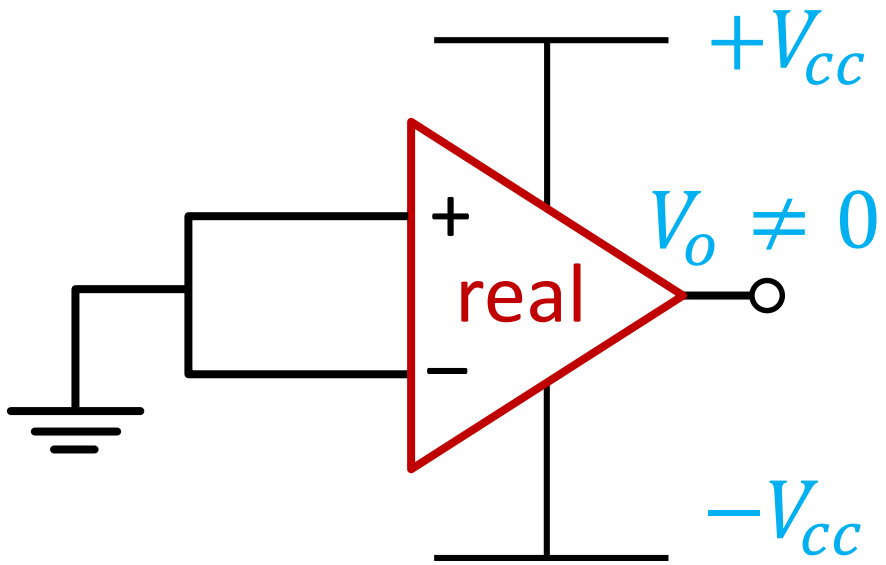
- In an ideal, symmetric OA,
$$V^+ = V^- = 0 \Rightarrow I_1 = I_2 \Rightarrow V_o = 0$$
- In a real OA, $I_1 \neq I_2 \Rightarrow V_o \neq 0$
- A small differential voltage V_{OS} must be applied to bring V_o to zero

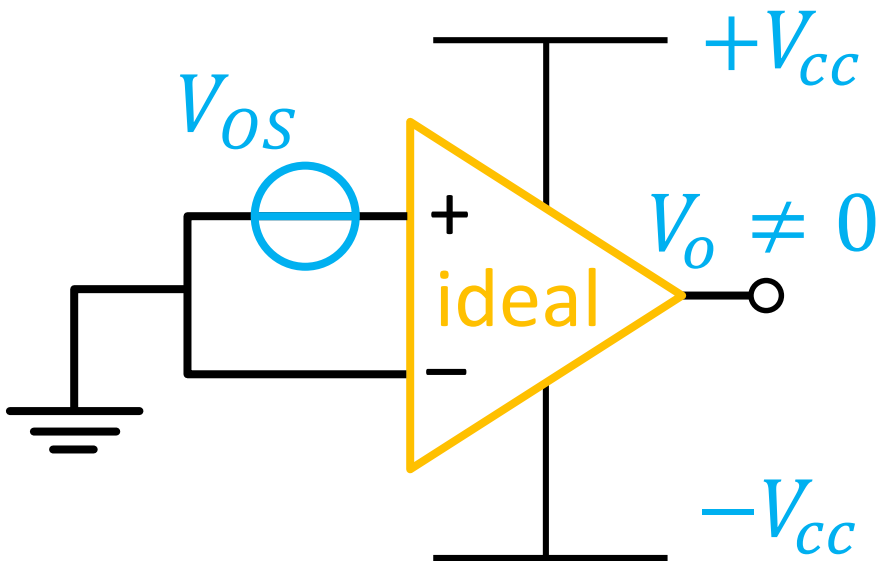
Technology dependence



	BJT	MOS	JFET/BiFET
ΔI	small	large	large
g_m	large	small	small
$\Delta V_{T/P}$	0	fair	large
V_{OS}	small	fair	large

Offset voltage modeling and value





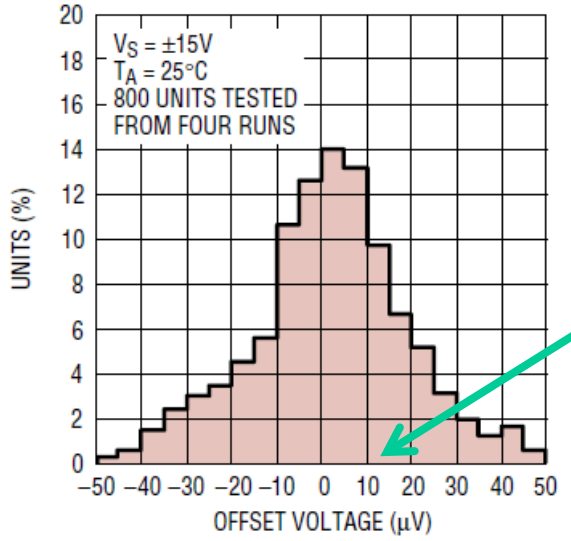
	best	typ
BJT OAs	$10 - 25\ \mu V$	$150\ \mu V - 10\ mV$
MOS OAs	$< 100\ \mu V - 1\ mV$	$200\ \mu V - 10\ mV$
JFET OAs	$100\ \mu V - 1\ mV$	$800\ \mu V - 15\ mV$

Offset voltage drift

- Describes the temperature dependence of V_{OS} (sometimes labelled as TCV_{OS})
- Typical values for general-purpose OAs are $1 - 10$ µV/°C
- Low-drift OAs have $dV_{OS}/dT < 0.3$ µV/°C

- «Chopper-stabilized» or «auto-zero» OA feature $V_{OS} < 1$ µV and $dV_{OS}/dT < 30$ nV/°C (more on this on the last lesson)

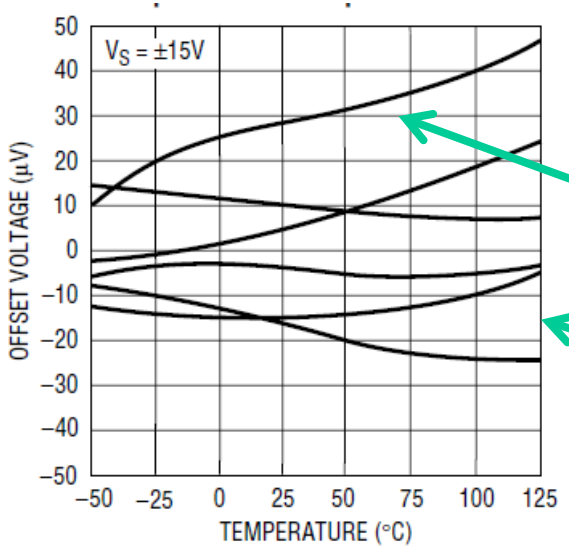
Actual values from datasheets



Scale=10 µV/div

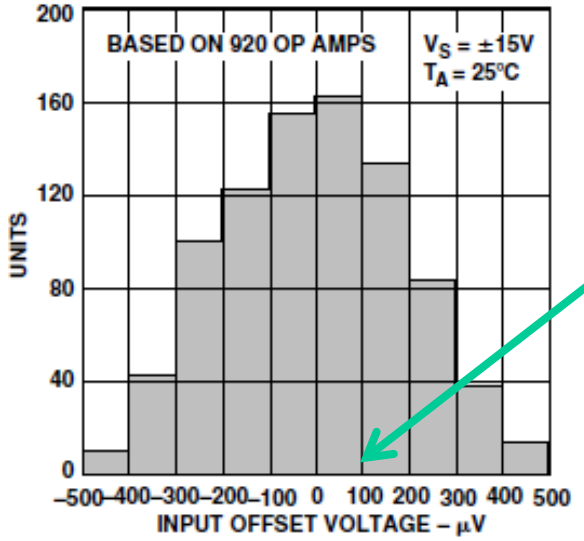
BJT,

precision



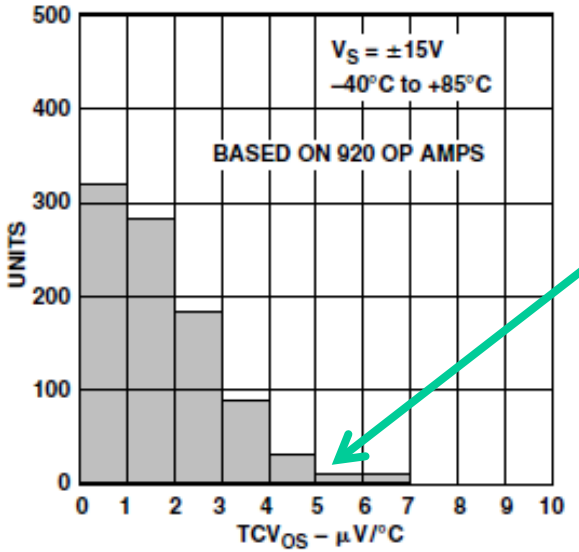
40 µV over 175°C
⇒ 0.23 μV/°C

Each device is different!



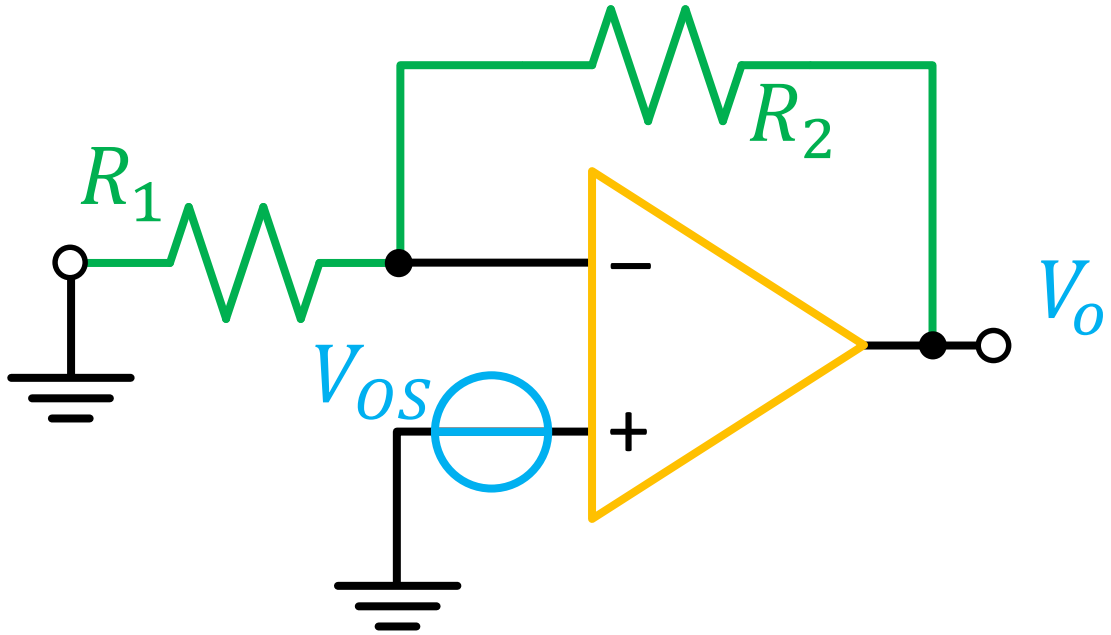
Scale=100 µV/div

JFET



A few µV/°C

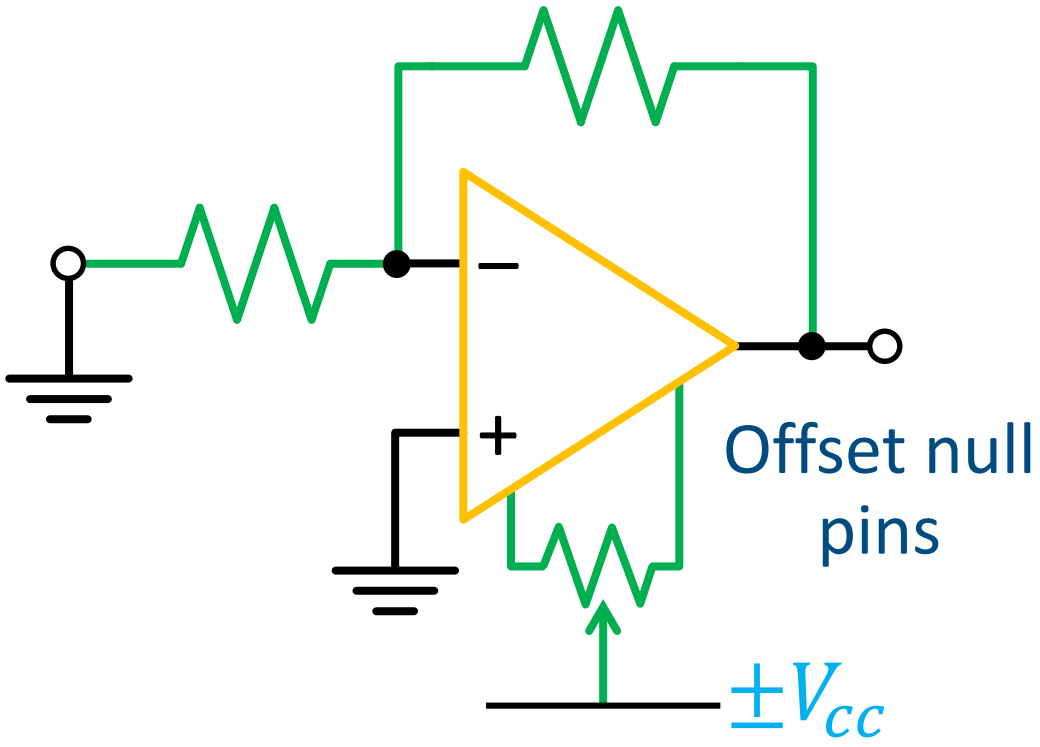
Output voltage



$$V_o = V_{OS}\frac{R_1 + R_2}{R_1}$$

Same values for I and NI amplifiers

Offset compensation

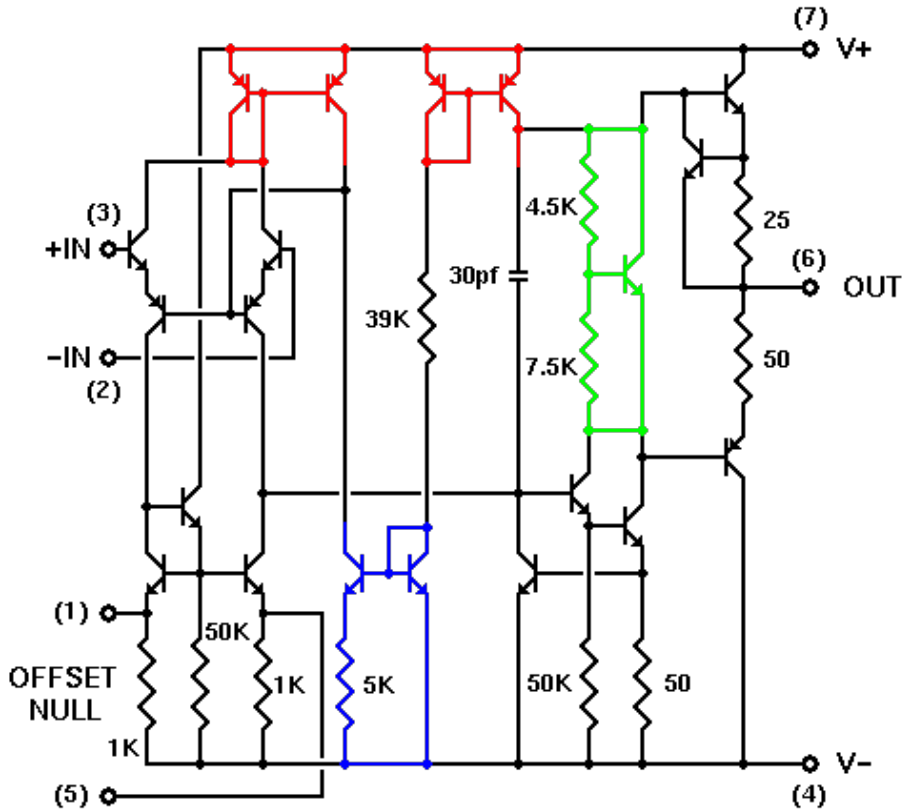


- Detailed compensation scheme provided by manufacturer
- Other schemes may be devised, i.e., biasing V^+ to get $V_o = 0$
- Obviously, drift or long-term stability cannot be compensated this way!

Outline

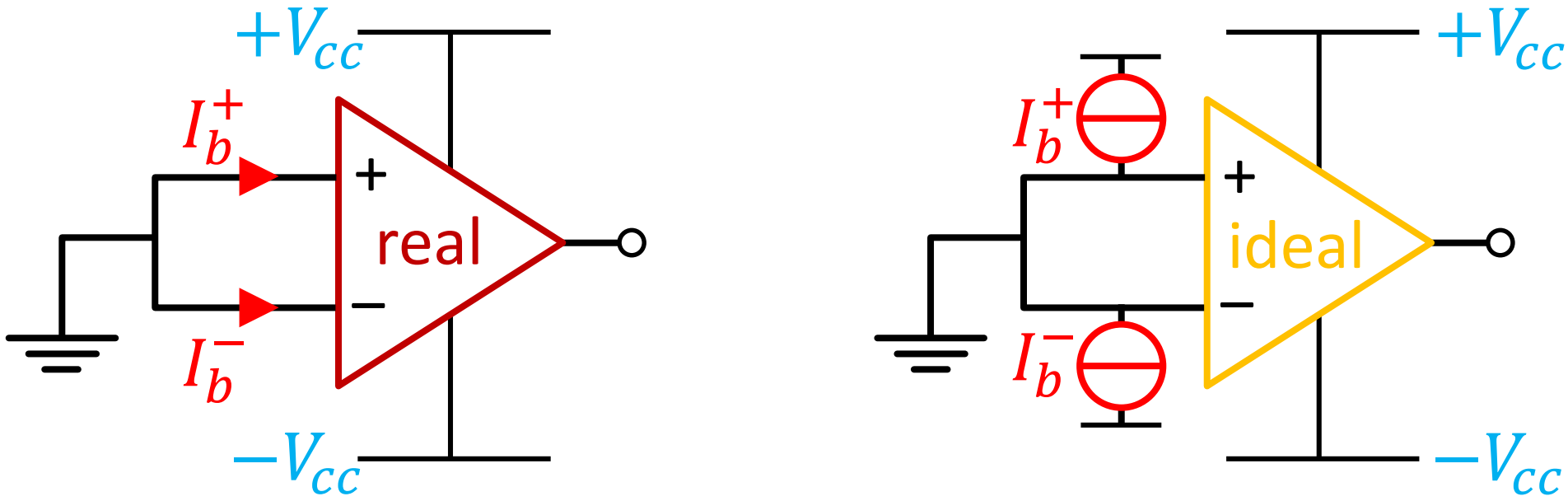
- Offset voltage
- Bias currents
- Effect on linear circuits

Input bias current



- BJTs in input stage require a DC base current I_b
- JFETs as input devices have reverse-biased *p-n* junctions
- MOSFETs have ESD protection circuits (diodes) which determine I_b

Bias current modeling



- Typ. BJT OA: $10^{-8} - 10^{-6}$ A
- Typ. JFET OA: $10^{-13} - 10^{-10}$ A
- Typ. CMOS OA: $10^{-13} - 10^{-10}$ A (ESD circ.)

Input offset current

- Bias currents at the two inputs are actually different, I_b^+ and I_b^-
- I_b is defined as their *average* value

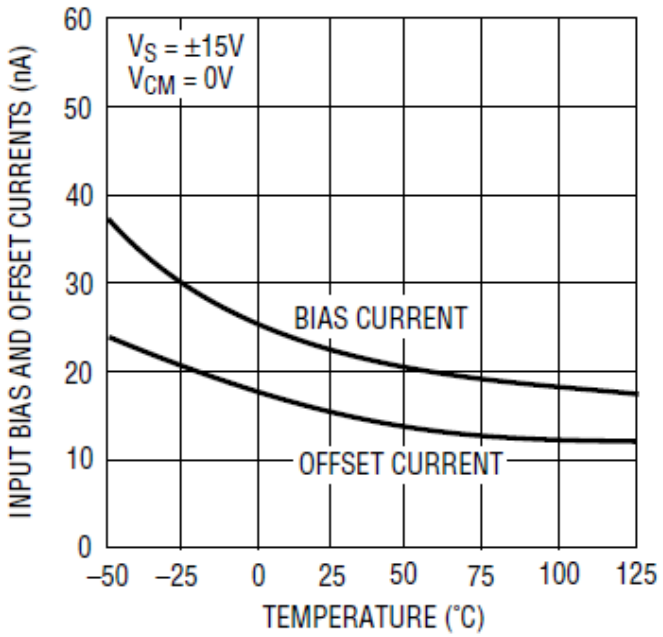
$$I_B = \frac{I_b^+ + I_b^-}{2}$$

- Offset current is defined as $I_{OS} = \left| I_b^+ - I_b^- \right|$
- Usually, an order of magnitude smaller than I_b

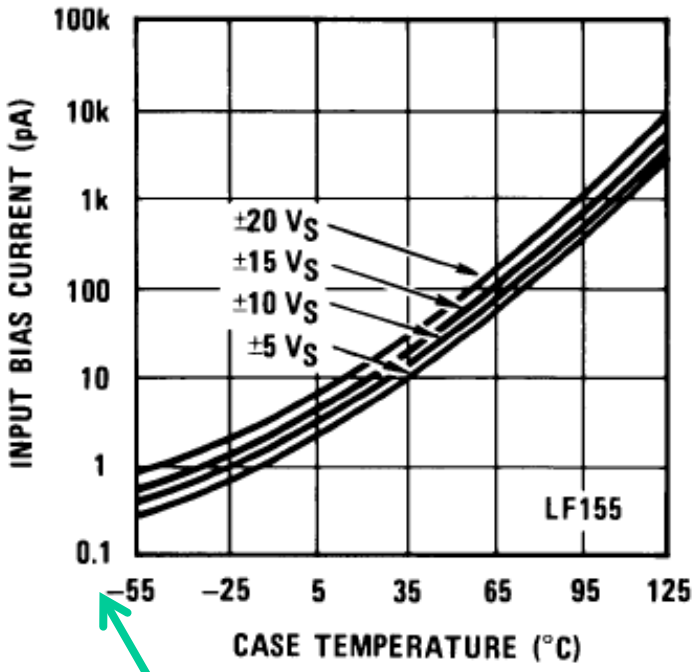
Bias and Offset current drift

- In FET and CMOS OAs, I_b and I_{OS} increase by a factor of two every $10°C$ (reverse currents of *p-n* junctions) $\Rightarrow$ check T range if low current is needed!
- BJT OAs usually have lower drifts ($10 - 100$ pA/°C)

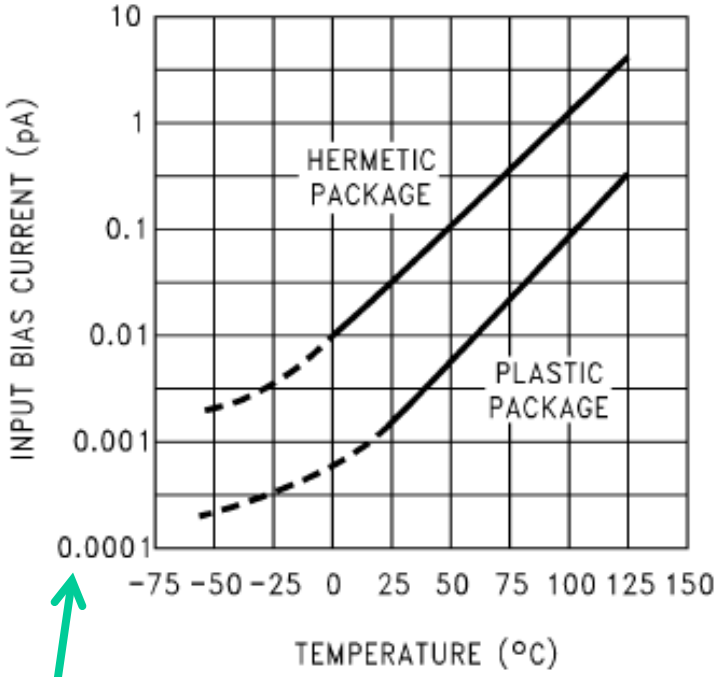
Actual values from datasheets



BJT



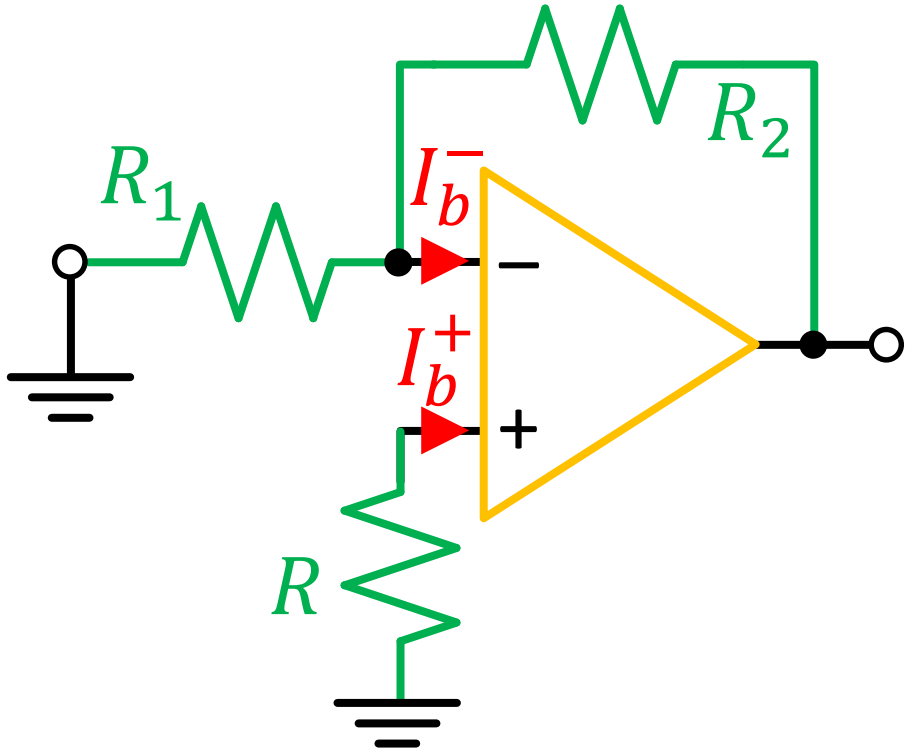
JFET



CMOS

Log scales ⇒ Exponential dependence!

Bias current compensation



$$V_o = I_b^- R_2 - I_b^+ R\left(\frac{R_1 + R_2}{R_1}\right)$$

$$= I_b R_2\left(1 - \frac{R}{R_1 \parallel R_2}\right)$$

$$+ I_{OS}\frac{R_2}{2}\left(1 + \frac{R}{R_1 \parallel R_2}\right)$$

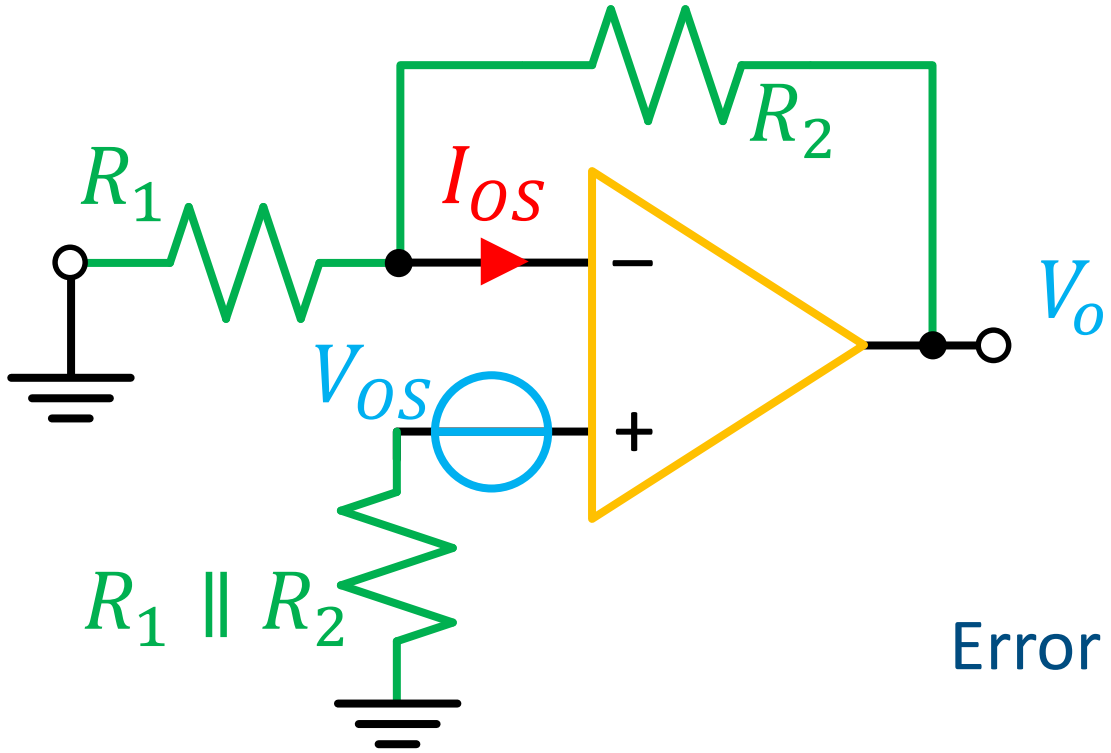
If $R = R_1 \parallel R_2$, I_b is compensated and $V_o = I_{OS}R_2$

(only useful if $I_{OS} \ll I_b$)

Outline

- Offset voltage
- Bias currents
- Effect on linear circuits

Total error – inverting amplifier

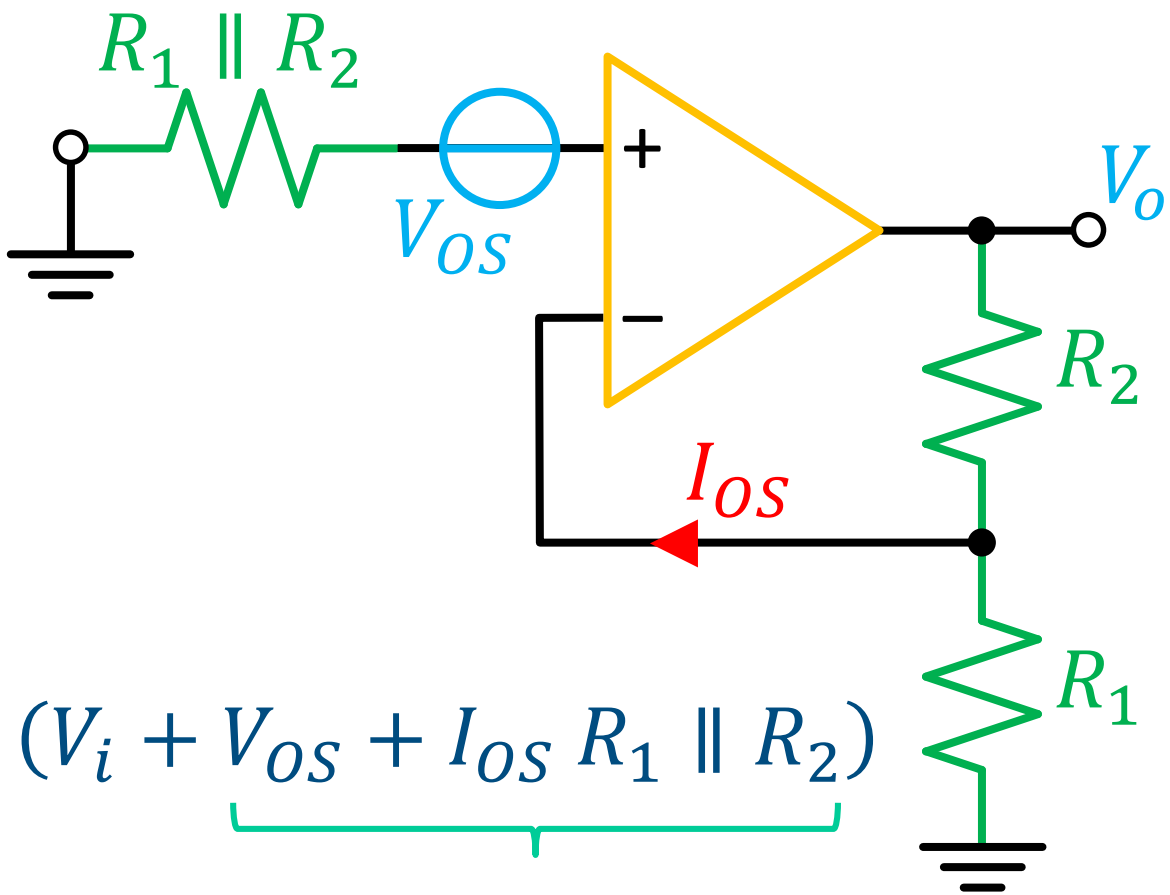


If I_b is compensated, symmetry allows to place just one I_{OS} source

Error (trade-off with $R_{in} = R_1$)

$$V_o = -\frac{R_2}{R_1}\left(V_i + V_{OS}\frac{R_1 + R_2}{R_2} + I_{OS}R_1\right)$$

Total error – non-inverting amplifier



$$V_o = \frac{R_1 + R_2}{R_1}\left(V_i + \underbrace{V_{OS} + I_{OS}\, R_1 \parallel R_2}_{\text{Error}}\right)$$