Electronics - Tutorage 1

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Review of feedback theory

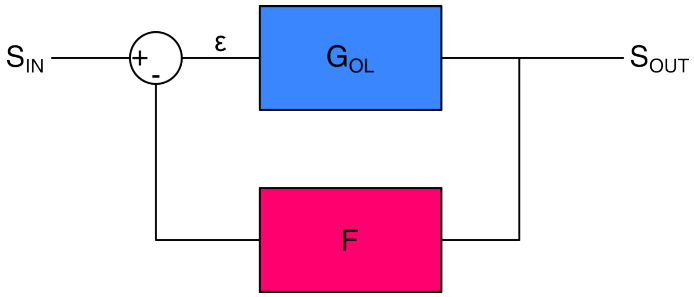

Figure 1: Block diagram of a generic negative feedback system.

List of useful relations:

- $G_{loop} = -F \cdot G_{ol}$
- $G_{id} = 1/F$
- $G = \frac{S_{out}}{S_{in}} = \frac{G_{ol}}{1+F \cdot G_{ol}} = \frac{G_{id}}{1-1/G_{loop}}$

The stage gain can be approximated as:

- $G = G_{id}$ if $|G_{loop}| \gg 1$
- $G = G_{ol}$ if $|G_{loop}| \ll 1$

I/O impedances calculation

I/O impedances can be calculated, in a general negative feedback system, following the procedure:

a. Calculate the ideal I/O impedance Z_{id}

b. Calculate the open-loop impedance Z_{ol}

c. Calculate G_{loop}

Once this has been done, the I/O impedance can be calculated as:

- $Z_{I/O} = Z_{ol} \cdot (1 - G_{loop})$ if $|Z_{id}| = \infty$
- $Z_{I/O} = Z_{ol}/(1 - G_{loop})$ if $|Z_{id}| = 0$

Calculating Z_{id}

To calculate the ideal impedance it is possible to proceed with the calculations by considering the OA ideal and with infinite gain. This implies that there exist a virtual short-circuit between the OA input terminals. Then, to evaluate then the ideal impedance, we can disconnect all the sources and connect an appropriate test source to the desired terminal. The evaluation of the reciprocal test quantity provides the ideal impedance as $Z_{id} = V_T/I_T$. Note that the test source has to be chosen wisely to avoid the necessity of introducing OA non-idealities.

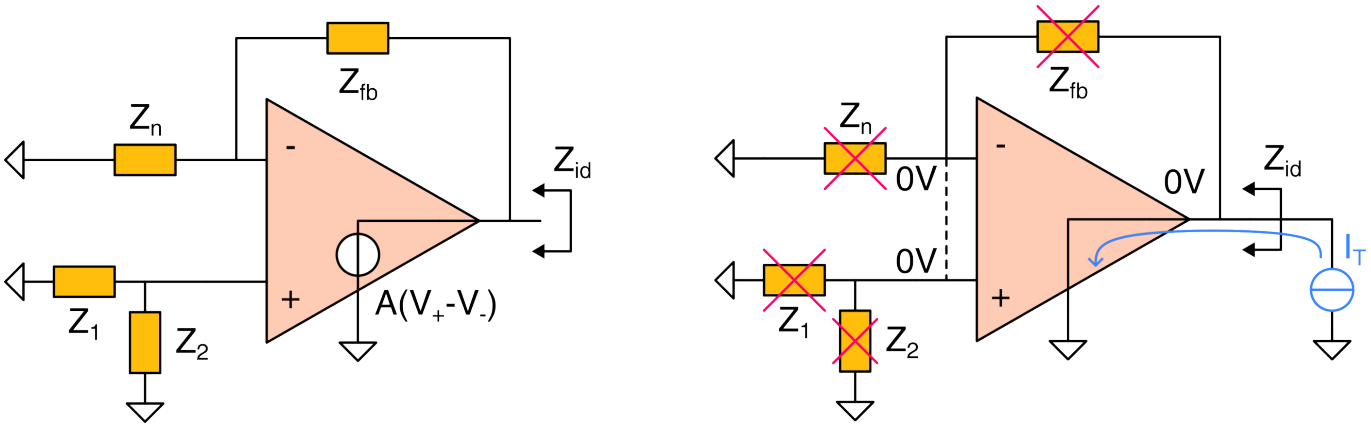

Figure 2: Example of the calculations to perform in order to evaluate the impedance seen, in this case, from the output node of an OA stage. The figure on the right highlights that, by employing a current test source, the impedance calculation is straightforward.

As an example, in Figure 2 we are trying to calculate the output impedance of an OA stage. The positive input of the OA stage is kept at ground, as current cannot flow from the input terminal of the OA. Thanks to the infinite gain of the stage, also the negative input terminal is kept at ground and thus no current flows in Z_n. Without any available path, current cannot flow along Z_{fb} and the output is forced to ground. If we probe the output impedance with a voltage source, directly connecting it to the output terminal, we would end up in a situation where the node is kept at ground by the infinite gain of the OA and at V_T from the test voltage source. As the connection is expected to have no impedance, an infinite current is required to flow, resulting in $Z_{id} = 0$. Although the result is correct, the reasoning is a little tricky. To avoid this situations, a good choice would have been to employ a current source: in that case, the current flows through the OA output, seeing null impedance, and Z_{id} is correctly evaluated as 0. As a general reference, if we expect a node to have ∞ impedance, the good choice for the test source is a voltage source, while for a 0 impedance node a good choice is to use a current source.

Calculating Z_{ol}

In most of the cases of interest, the calculation of G_{ol} can be safely performed by simply not considering the OA action while testing the circuit from the desired terminal. In some cases, OA internal impedances, as the differential impedance Z_d or the output resistance R_o, may have to be considered in order to avoid trivial results, *i.e.* $Z_{I/O} = 0$ or $Z_{I/O} = \infty$.

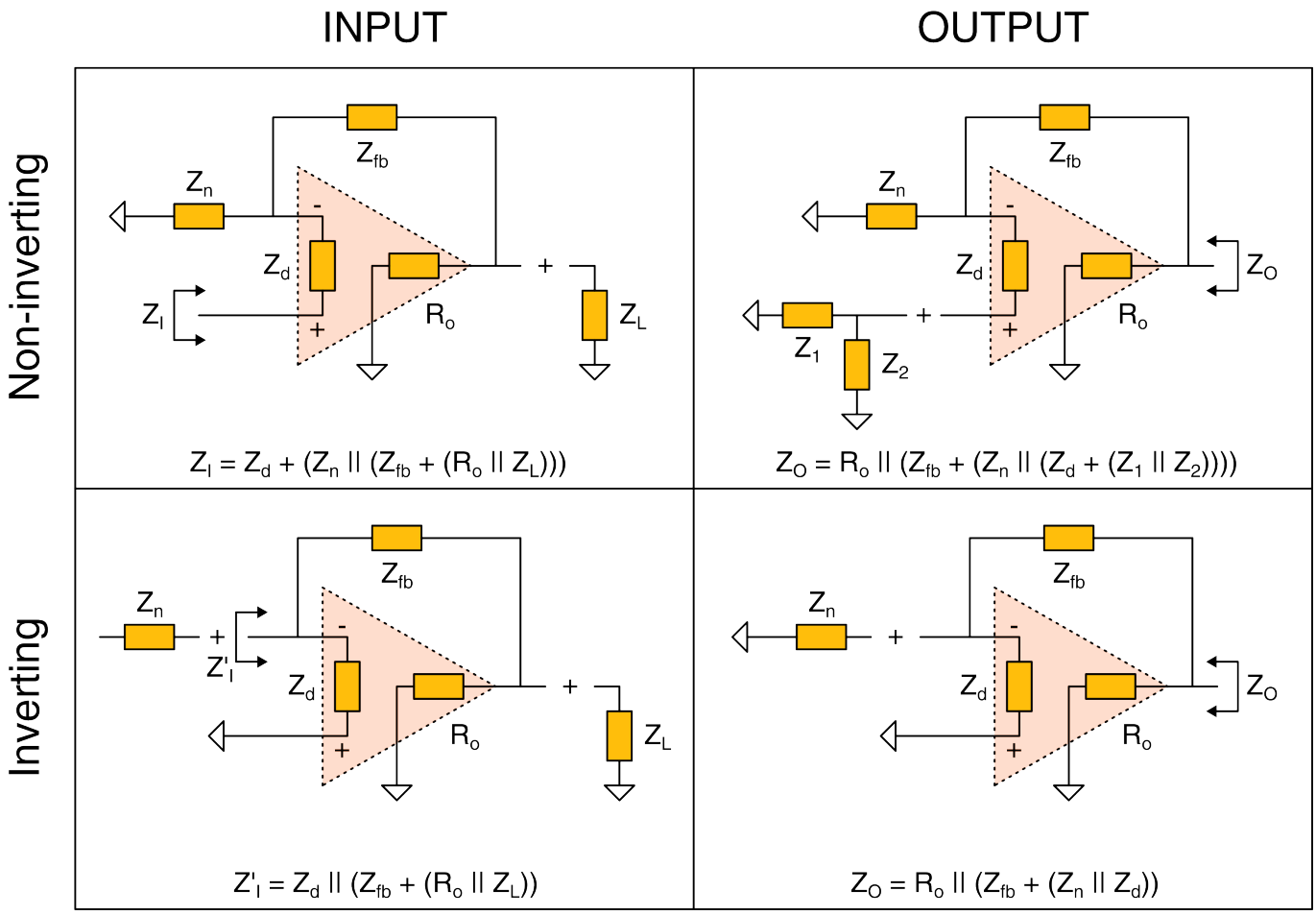

Figure 3: Table summarizing the calculation of the open loop impedance Z_{ol} in the most typical cases of interest.

- Non-inverting conf., Z_I: the output resistance R_o slightly increases the open-loop impedance but also makes it dependent on the load. The differential impedance provides a significant contribution to the overall result (except for very high frequencies).
- Inverting conf., Z_I: the differential impedance has a minimal role at low frequencies, being in parallel with a branch that usually provides a smaller impedance path. The output resistance has the same effect as in the non-inverting configuration.
- Non-inverting conf., Z_O: the output resistance is necessary, otherwise the overall Z_{ol} would have been null. The differential impedance has a small impact if Z_n is sufficiently smaller than Z_d.
- Inverting conf., Z_O: same as in the non-inverting configuration.

Calculating G_{loop}

The calculation for the loop-gain can be performed exactly in the same way as it is done when it comes to calculate the real gain of the OA stage. Being a global property of the feedback system, G_{loop} is independent from the point of the circuit in which it is evaluated. To calculate G_{loop} the procedure to follow is:

a. Turn off any voltage/current source

b. Cut the loop at a chosen node

c. Reconstruct, if needed, impedance!

d. Connect a test generator and calculate the transfer function

Although what previously said on the freedom in the choice of the break point, there are certainly some smart nodes where cutting is preferable. These are all the points in which impedance reconstruction is not needed, *i.e.* nodes where the impedance is infinite or nodes that are driven by an ideal voltage source. In this category falls:

- Inverting input of the OA, when it is not specifically asked to consider the differential impedance
- OA output, when it is not specifically asked to consider the output resistance

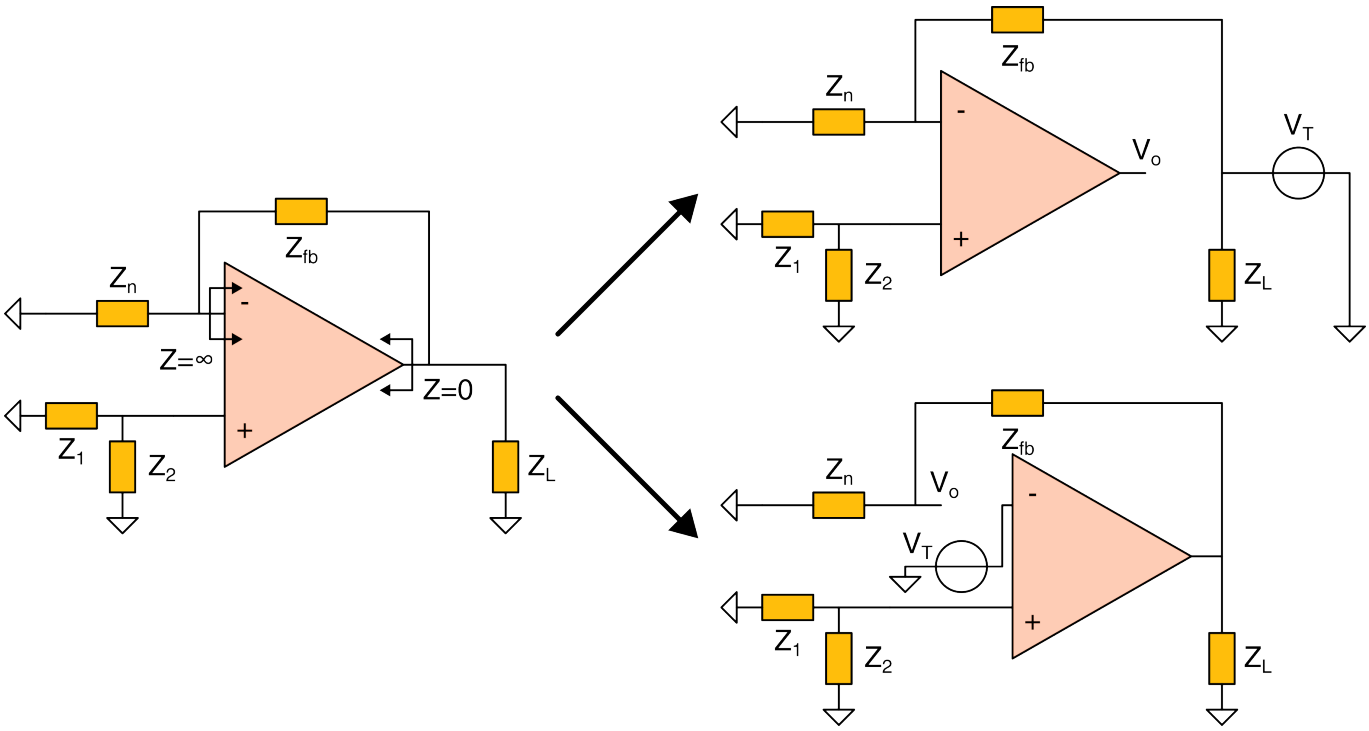

Figure 4: Example of the calculations that are needed to evaluate G_{loop}. The figure highlights two possible nodes where cutting the loop is extremely convenient, as impedance reconstruction is not needed.

Exercise - Virtual inductance

Discrete inductors are usually very large components. Figure 5(a) shows an example of a $1mH$ inductor highlighting the component dimensions. Moreover, from the perspective of integrated circuits, inductances of very large value are typically very hard to be designed. For this reason, circuit designer often prefer different choices when an inductor is needed. A possible way to proceed is to implement the so-called virtual inductance, whose schematic is reported in Figure 5(b). This configuration exploits the OA feedback to manipulate the impedance seen from the input terminal, resembling the behavior of an inductance to ground.

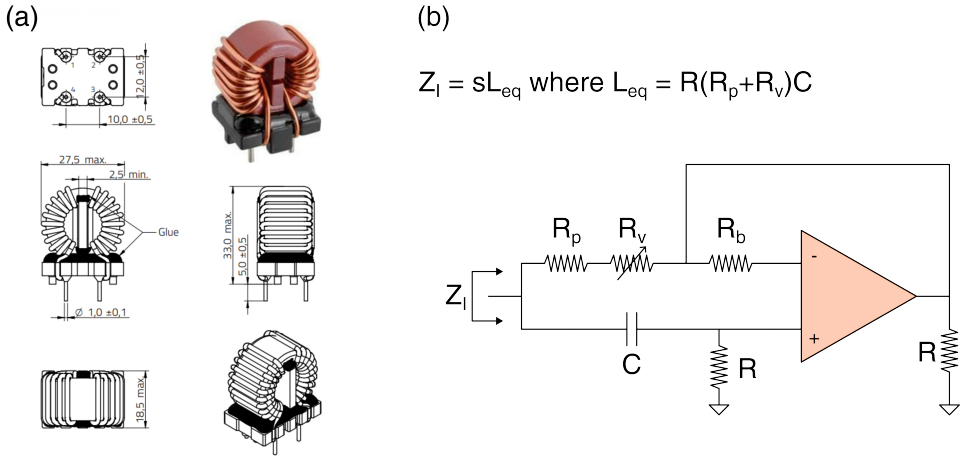

Figure 5: (a) Example of the dimensions of a $1mH$ inductor, from datasheet (744824101, Wurth Elektronik). (b) Scheme of a virtual inductance circuit exploiting an OA stage to mimic an inductor to ground.

The circuit thus realized can be implemented with only capacitors and resistances, which are much more easier to deal with during the design stage. The variable resistor R_v can be used to tune the virtual inductance value while the resistor R_p, in series to R_v, serves the scope of avoiding a short-circuit between input and OA output when $R_v = 0\Omega$.

The student is asked to calculate the ideal input impedance Z_I, showing under which assumptions the reported result is correct.

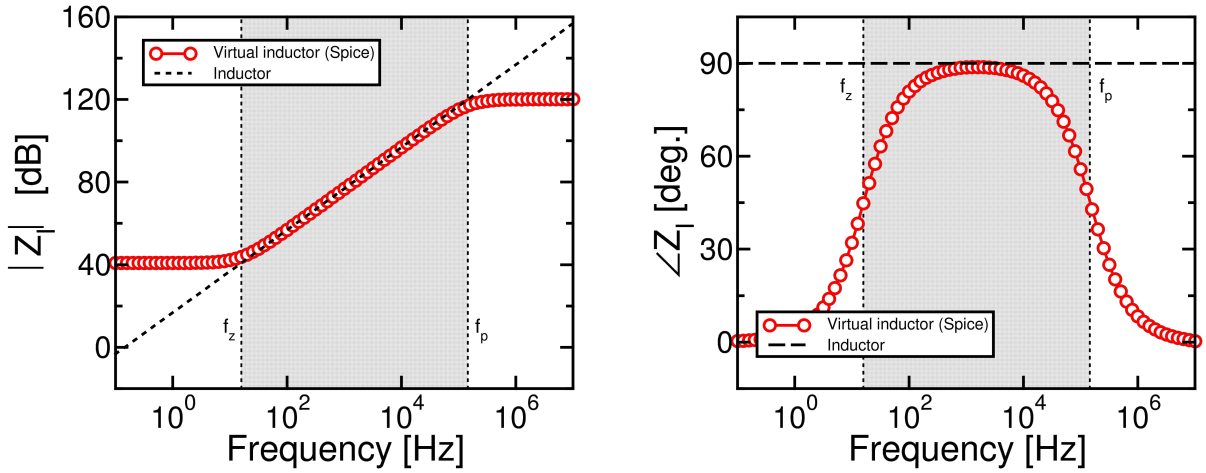

Figure 6: Magnitude (left) and Phase (right) Bode diagram of the virtual inductance stage.

The circuit shown in Figure 5(b) was simulated with the help of a Spice simulator and results are shown in Figure 6. Virtual inductance components values are $C = 10nF$, $R = 1M\Omega$, $R_p = 10\Omega$ and $R_v = 100\Omega$. The expected virtual inductance value is of $1.1H$. Note that in the frequency range between $f_z = 16Hz$ and $f_p = 145kHz$ the behavior of the virtual inductance circuit well approximates the one of an inductor of equivalent value.

Exercise - Howland current pump

The configuration that we are going to study in this exercise was invented by MIT's Professor Bradford Howland in the early 1960s, with the aim of designing a stage capable of driving current-hungry loads. Indeed, driving a small impedance load, for example a 200Ω resistance, is typically a difficult task due to the current needed to impose the correct bias. A voltage source would not be ideal to drive it, due to the non-zero series resistance which inevitable would lead to an important partition of the provided voltage. At the same time, providing the driving voltage through a buffer stage might be problematic in contexts where high-performance are required: op-amps typically trade-off between high performance, *i.e.* low offset voltage, low offset current and low distortion, and driving capabilities, so that it is difficult nor impossible sometimes to find a device capable of satisfy all the requirements.

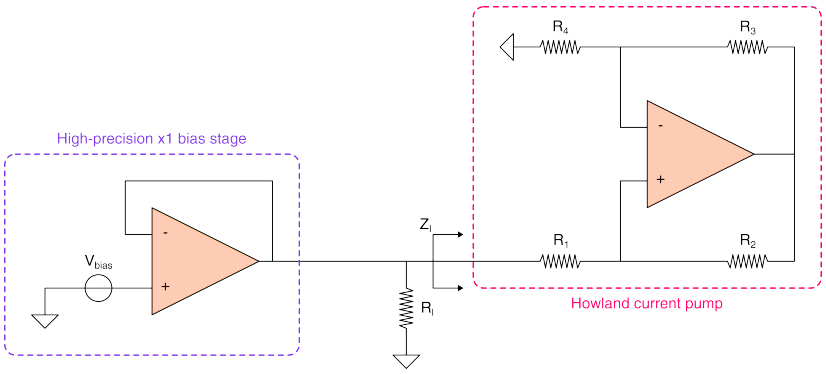

Figure 7: Example of a circuit in which the Howland current pump is employed to supply the current needed to drive the load R_L. In the circuit, the unity-gain high-performance stage provide the bias to the load..

The idea behind the Howland current pump is to drive the low-impedance load with a high-performance stage, which thus satisfy the requirements in terms of offset and distortion, finding a way to *cancel* the low-impedance load burden by making it looks like an infinite-impedance load. The first step to take is to understand that a load Z can be made infinite or zero if we place, respectively, in parallel or in series a load of equal $|Z|$ but of opposite sign. Let's suppose that the load is purely resistive: then it is just a matter of designing a stage whose input impedance is a negative resistance! Although weird, this can be accomplished with the simple OA configuration shown in Figure 7.

The student is asked to calculate the circuit G_{id} and G_{loop}, finding the condition for which the overall feedback is negative. Then, calculate the ideal input impedance Z_I, finding the conditions on resistances R_1, R_2, R_3 and R_4 which allow to remove completely the effect of a load R_L driven by a high-performance stage.

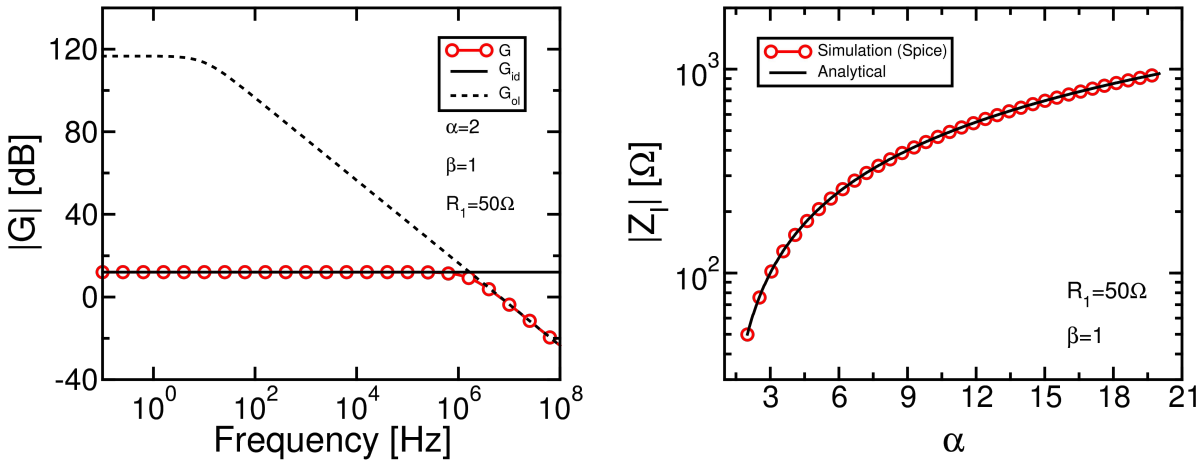

Figure 8: (Left) Real gain of the Howland current pump from input to OA output terminal. OA characteristics are $A_0 = 10^6$ and $GBWP = 10^7$. Resistor values are $R_1 = 50\Omega$, $R_2 = R_3 = R_4 = 100\Omega$. $\alpha = R_2/R_1$ and $\beta = R_3/R_4$. (Right) Absolute value of the static (negative) input impedance of the Howland stage.

List of relevant exams

- Exam of 11$^{\text{th}}$ September 2015, exercise 1 (Q.4)
- Exam of 14$^{\text{th}}$ September 2017, exercise 1 (Q.4)
- Exam of 20$^{\text{th}}$ July 2018, exercise 1 (Q.2 and Q.4)
- Exam of 23$^{\text{rd}}$ June 2021, exercise 1 (Q.4)
- Exam of 19$^{\text{th}}$ June 2024, exercise 1 (Q.1)